Anand Sivasubramaniam

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Research Interests

Computer Architecture, Parallel Processing, Operating Systems,
Simulation and Evaluation of Computer Systems.

Academic Record

Graduate (1989-the present)

Working towards a PhD in Computer Science at
Georgia Institute of Technology, Atlanta, GA 30332.
Expected Graduation: June 1995 (Defense completed)
Thesis: A Framework for Evaluating Architectural Issues of Parallel Systems.

Thesis Committee:	Dr. Umakishore Ramachandran (chairman)
	Dr. H. Venkateswaran (co-advisor)
	Dr. Richard M. Fujimoto
	Dr. Sudhakar Yalamanchili
	Dr. Mark D. Hill (Univ. of Wisconsin, Madison)

Graduate (1989-1991)

Master Of Science (MS) in Computer Science at
Georgia Institute of Technology, Atlanta, GA 30332.

Undergraduate (1985-1989)

Bachelor Of Technology (B.Tech) in Computer Science at
Indian Institute of Technology, Madras 600036, India.

Work Experience

January 1993 - the present

Research Assistant at the College of Computing,
Georgia Institute of Technology, Atlanta, GA 30332.
Project: Top-down Approach to Scalability Study of Parallel Systems.

June 1992 - December 1992

Software Engineer in the Massively Parallel Systems Group,
Digital Equipment Corporation, Maynard, MA 01754.
Project: Designing and evaluating communication mechanisms for
Alpha AXP Workstations connected by high-speed networks (ATM and FDDI).

September 1989 - June 1992

Teaching Assistant at the College of Computing,
Georgia Institute of Technology, Atlanta, GA 30332.

Publications

1. A. Sivasubramaniam, A. Singla, U. Ramachandran, H. Venkateswaran. A Simulation-based Scalability Study of Parallel Systems. **Journal of Parallel and Distributed Computing**, 22(3):411-426, September 1994.
2. A. Sivasubramaniam, A. Singla, U. Ramachandran, H. Venkateswaran. On Characterizing Bandwidth Requirements of Parallel Applications. To appear in **Proceedings of the ACM SIGMETRICS Conference on Measurement and Modeling of Computer Systems**, May 1995.
3. A. Sivasubramaniam, A. Singla, U. Ramachandran, H. Venkateswaran. An Approach to Scalability Study of Shared Memory Parallel Systems. In **Proceedings of the ACM SIGMETRICS Conference on Measurement and Modeling of Computer Systems**, pages 171-180, May 1994.
4. A. Sivasubramaniam, A. Singla, U. Ramachandran, H. Venkateswaran. Abstracting Network Characteristics and Locality Properties of Parallel Systems. In **Proceedings of the First International Symposium on High Performance Computer Architecture**, pages 54-63, January, 1995.
5. A. Sivasubramaniam, G. Shah, J. Lee, U. Ramachandran, H. Venkateswaran. Experimental Evaluation of Algorithmic Performance on Two Shared Memory Multiprocessors. In N. Suzuki, editor, **Shared Memory Multiprocessing**, pages 81-107, MIT Press, 1992. {Also appeared in **Proceedings of the First International Symposium on Shared Memory Multiprocessing**, April 1991.}
6. A. Sivasubramaniam, U. Ramachandran, H. Venkateswaran. A Computational Model for Message-Passing. In **Proceedings of the Sixth International Parallel Processing Symposium**, March 1992.
7. U. Ramachandran, H. Venkateswaran, A. Sivasubramaniam, A. Singla. Issues in Understanding the Scalability of Parallel Systems. In **Proceedings of the First International Workshop on Parallel Processing**, pages 399-404, December 1994.
8. with I. Yanasak et al. Parallelizing Sequential Algorithms for the Generalized Assignment Problem. In **Proceedings of the DIMACS Implementation Challenge Workshop**, October, 1994.
9. U. Ramachandran, H. Venkateswaran, A. Sivasubramaniam. A Top-down Approach to the Scalability Study of Shared Memory Multiprocessors. In the **Second Workshop on Scalable Shared Memory Multiprocessors** (held in conjunction with ISCA '91), May 1991.
10. A. Sivasubramaniam, U. Ramachandran, H. Venkateswaran. A Comparative Evaluation of Techniques for Studying Parallel System Performance. Technical Report GIT-CC-94/38, College of Computing, Georgia Institute of Technology, Atlanta, GA 30332. September, 1994. *Submitted for Publication*.
11. U. Ramachandran, G. Shah, A. Sivasubramaniam, A. Singla, I. Yanasak. Architectural Mechanisms for Explicit Communication in Shared Memory Multiprocessors. Technical Report GIT-CC-94/59, College of Computing, Georgia Institute of Technology, Atlanta, GA 30332. December, 1994. *Submitted for Publication*.
12. A. Sivasubramaniam, U. Ramachandran, H. Venkateswaran. Message-Passing: Computational Model, Programming Paradigm and Experimental Studies. Technical Report GIT-CC-91/11, College of Computing, Georgia Institute of Technology, Atlanta, GA 30332. February, 1991.

Academic Achievements

- Winner of the 1995 Graduate Research Assistant award in the College of Computing at Georgia Tech for outstanding research assistance in computer science.
- Participated in the 1991 Summer Institute on Parallel Computing at Argonne National Laboratory (25 students selected nationwide).
- Admitted with financial support for a Course on the Structure of Parallel Machines at Fibonacci Institute, Italy, in 1991 (10 students selected worldwide with financial support).
- Member of a team that developed a Multilingual Spreadsheet which was awarded the First Prize at the Annual Computer Society of India Convention (CSI-88).
- Recipient of National Talent Search Scholarship (a prestigious undergraduate fellowship).
- All India 39th Rank (out of 80,000) in the Joint Entrance Examination to the Indian Institute of Technology.
- 1st Rank in the All India Senior School Certificate Examination (60,000 examinees).
- Winner of Major General Virendra Singh Gold Medal for standing first in Mathematics in India (1985).

Technical Skills

- Systems programming skills for implementing communication mechanisms across networked workstations, device drivers, and other kernel-level code used in operating systems development, with proficiency in C, C++.
- Extensive experience in parallel programming on machines like the KSR-1, Sequent Symmetry, BBN Butterfly, Intel Paragon, Intel iPSC/860, MasPar MP-2, networked workstations running PVM, and implementing applications on these machines.
- Good understanding of the issues involved in the architectural design of shared memory and message passing multiprocessors.
- Expertise in evaluating computer systems using simulation packages such as CSIM, SMPL.

Educational Activities

- Assisted in teaching graduate and undergraduate level courses in Computer Architecture.
- Generation and supervision of class projects for computer architecture courses. Many of these projects evolved from issues related to my thesis. For instance, the SPASM multiprocessor simulator, an integral contribution of my thesis, was an invaluable educational tool in helping students comprehend details of parallel architectures and writing performance conscious programs for them. Students implemented applications on the simulator and used the detailed statistics to understand the performance of their implementations and to even improve them. More advanced projects focussed on extending SPASM itself for different network topologies.
- Helped prepare tutorial notes on 'Multigranular Computing' for Dr. Ramachandran which was presented at several conferences including ISCA '93, SIGMETRICS '94, ICPP '94.

Course Work

Courses completed at the graduate and undergraduate levels in the areas of Computer Architecture, Operating Systems, Databases, Algorithms & Data Structures, Programming Languages, Digital Design, and Automata Theory.

Thesis Abstract

Evaluating and analyzing the performance of a parallel application on an architecture to explain the disparity between projected and delivered performance is an important aspect of parallel systems research. But conducting such a study is hard due to the complex interaction between application characteristics and architectural features. Performance evaluation techniques have to grapple with several more degrees of freedom exhibited by these systems compared to their sequential counterparts. In order to be useful, the performance metrics quantified by these techniques should reveal sufficient information about the execution of the application. In this thesis, we present metrics and techniques used for evaluating parallel systems and discuss their relative merits and de-merits. We introduce a set of metrics called overhead functions for quantifying performance and develop a framework for studying parallel systems. At the heart of our evaluation framework lies an execution-driven simulator called SPASM (Simulator for Parallel Architectural Scalability Measurements) which isolates and quantifies the overhead functions over a range of hardware platforms. We illustrate the use of the framework for investigating different architectural issues in parallel systems research. In the first, we study the scalability of parallel applications on shared memory and message-passing hardware platforms. In the second study, we illustrate the use of the framework in evaluating the validity of theoretical/analytical models that are used for abstracting features of parallel systems. In the third study, we illustrate its use in synthesizing architectural requirements of parallel applications, in particular, we focus on the interconnection network and characterize the bandwidth requirements. Finally, assimilating the information gleaned from the different studies in this thesis, we identify types of communication typically found in applications and propose a set of architectural mechanisms that help reduce the communication overhead.

References

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2. Dr. H. Venkateswaran, Associate Professor, College of Computing,
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   venkat@cc.gatech.edu

3. Dr. Sudhakar Yalamanchili, Associate Professor, Electrical and Computer Engineering,
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4. Dr. Marco Annaratone, Technical Director, High Performance Computing,
   Digital Equipment Corporation, 129 Parker Street, PK03-2, Maynard, MA 01754.
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5. Dr. Richard M. Fujimoto, Associate Professor, College of Computing,
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