65550

Video Capture Port

Application Note
Revision 1.1

February 1996

P R E L I M I N A R Y

Revision History

Revision	Date	By	Comment
0.1	5/26/95	EC/st	Draft - Internal Review
1.0	5/26/95	ST	Officical Release
1.1	2/7/96	LC	Removed confidential markings.

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Introduction

The 65550 provides a flexible interface that can be configured as a VAFC interface, Video Port or as a memory interface to an external frame buffer for STN-DD panel enhancement. Focusing on the Video Port option, the 65550's PC video interface is a uni-direction digital video input port that accepts 16-bit YUV data, two synchronizing signals HREF and VREF, and a pixel rate clock VCLK. Taking the digital video data from this video port, 65550 can perform video functions such as color space conversion, scaling, zooming, interpolation and video playback on a 24-bit TFT panel.

The YUV data input to the 65550 video capture port can be in RGB-15, RGB-16 or YUV 4:2:2 format. In YUV 4:2:2 format, eight data bits are allocated for Y (luminance) and eight data bits for UV (chrominance).

Signals

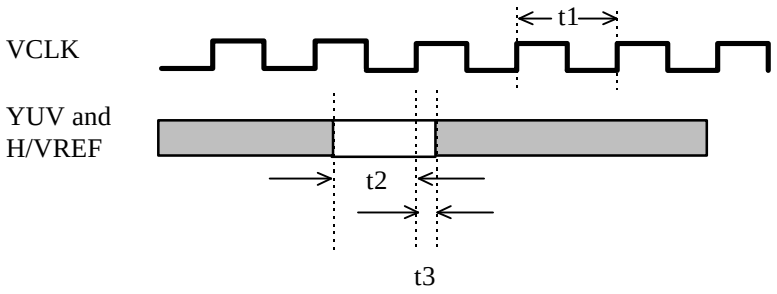
Y	(8 signals)	Luminance data channel
C(U/V):	(8 signals)	Chrominance data channel
HREF:	Horizontal blanking signal	
VREF:	Vertical sync signal	
VCLK:	Pixel clock for data and HREF and VREF	

All pixel and timing data are aligned to the rising edge of VCLK.

65550 Pin Assignments for Video Port interface

Pin #	Name	Type	Video port Name	Type
98	CA8	I/O	VREF	I
99	HREF	I/O	HREF	I
100	OEC#	I/O	VCLK	I
107	MCD1	I/O	Y0	I
109	MCD2	I/O	Y1	I
110	MCD3	I/O	Y2	I
111	MCD4	I/O	Y3	I
112	MCD5	I/O	Y4	I
113	MCD6	I/O	Y5	I
114	MCD7	I/O	Y6	I
115	MCD8	I/O	Y7	I
116	MCD9	I/O	UV0	I
117	MCD10	I/O	UV1	I
118	MCD11	I/O	UV2	I
120	MCD13	I/O	UV3	I
121	MCD14	I/O	UV4	I
122	MCD15	I/O	UV5	I
104	CASCL#	I/O	UV6	I
103	CASCH#	I/O	UV7	I

AC Timing



65550 Video Capture Port AC Specification

Symbol	Parameter	Min	Units
t1	VCLK period	62.5	nS
t2	YUV & H/VREF setup	10	nS
t3	YUV & H/VREF hold	2	nS

Registers Description

MRX: Index register IO address: 3D2h

All following registers are data registers with IO address '3D3h'

MR nn: where 'nn' is the Index value in hex

MR02: Acquisition control 1: R/W

- 0 Interlace
  - 0 Non-interlace (default)
  - 1 Interlace
- 1 Reserved
- 2 Data Format
  - 0 YUV (default)
  - 1 RGB
- 3 RGB Format (RGB only)
  - 0 RGB15 (default)
  - 1 RGB16
- 4 Hsync Polarity
  - 0 Active low (default)
  - 1 Active high
- 5 Vsync Polarity
  - 0 Active low (default)
  - 1 Active high
- 6 Field Detect Polarity
  - 0 Normal (default)
  - 1 Inverted
- 7 Field Detect Method
  - 0 Trailing edge of V (default)
  - 1 Leading edge of V

MR03: Acquisition control 2: R/W

- 0 Grab start/stop control
  - 0 Stop (default)
  - 1 Start
- 1 Continuous/Single
  - 0 Continuous (default)
  - 1 Single
- 2 Frame/Field Grab
  - 0 Frame (default)
  - 1 Field
- 3 Field
  - 0 Field 0 (default)
  - 1 Field 1
- 4 X Scale Enable
  - 0 Full screen (default)
  - 1 Scaled on H
- 5 Y Scale Enable
  - 0 Full Screen (default)
  - 1 Scale on V
- 7-6 V Scaling Method
  - 00 Normal (default)
  - 01 Reserved
  - 10 Reserved
  - 11 Reserved

MR04: Acquisition Control 3

- 0 X Capture Direction
  - 0 L to R (default)
  - 1 R to L
- 1 Y Capture Direction
  - 0 Top to bottom (default)
  - 1 Bottom to top
- 2 Horizontal Filter Enable
  - 0 No filter (default)
  - 1 Filter pixels with horizontal filter
- 3 Reserved
- 4 Double buffer enable
  - 0 Disable (default)
  - 1 Enable

5 Double Buffer Pointer
  0 Pointer 1
  1 Pointer 2
6 Reserved
7 Capture Counter Enable
  0 Capture single or continuous (default)
  1 Capture every 'n' field/frame as set in capture_frame-count

MR06: Acquisition Window pointer 1L 7-0

MR07: Acquisition Window pointer 1M 15-8

MR08: Acquisition Window pointer 1H 18-16 (3 bits)

MR09: Acquisition Window pointer 2L 7-0

MR0A: Acquisition Window po inter 2M 15-8

MR0B: Acquisition Window pointer 2H 18-16 (3 bits)

MR0C: Acquisition Window Width 7-0 (pixel_width/4: mem-quad words, scaled if enabled)

MR0E: Acquisition Window X Left LSB 7-0

MR0F: Acquisition Window X Left MSB 10-8 (3 bits)

MR10: Acquisition Window X Right LSB 7-0

MR11: Acquisition Window X Right MSB 10-8 (3 bits)

MR12: Acquisition Window Y Top LSB 7-0

MR13: Acquisition Window Y Top MSB 10-8 (3 bits)

MR14: Acquisition Window Y Bottom LSB 7-0

MR15: Acquisition Window Y Bottom MSB 10-8 (3 bits)

MR16: Acquisition Horizontal Scale 7-0

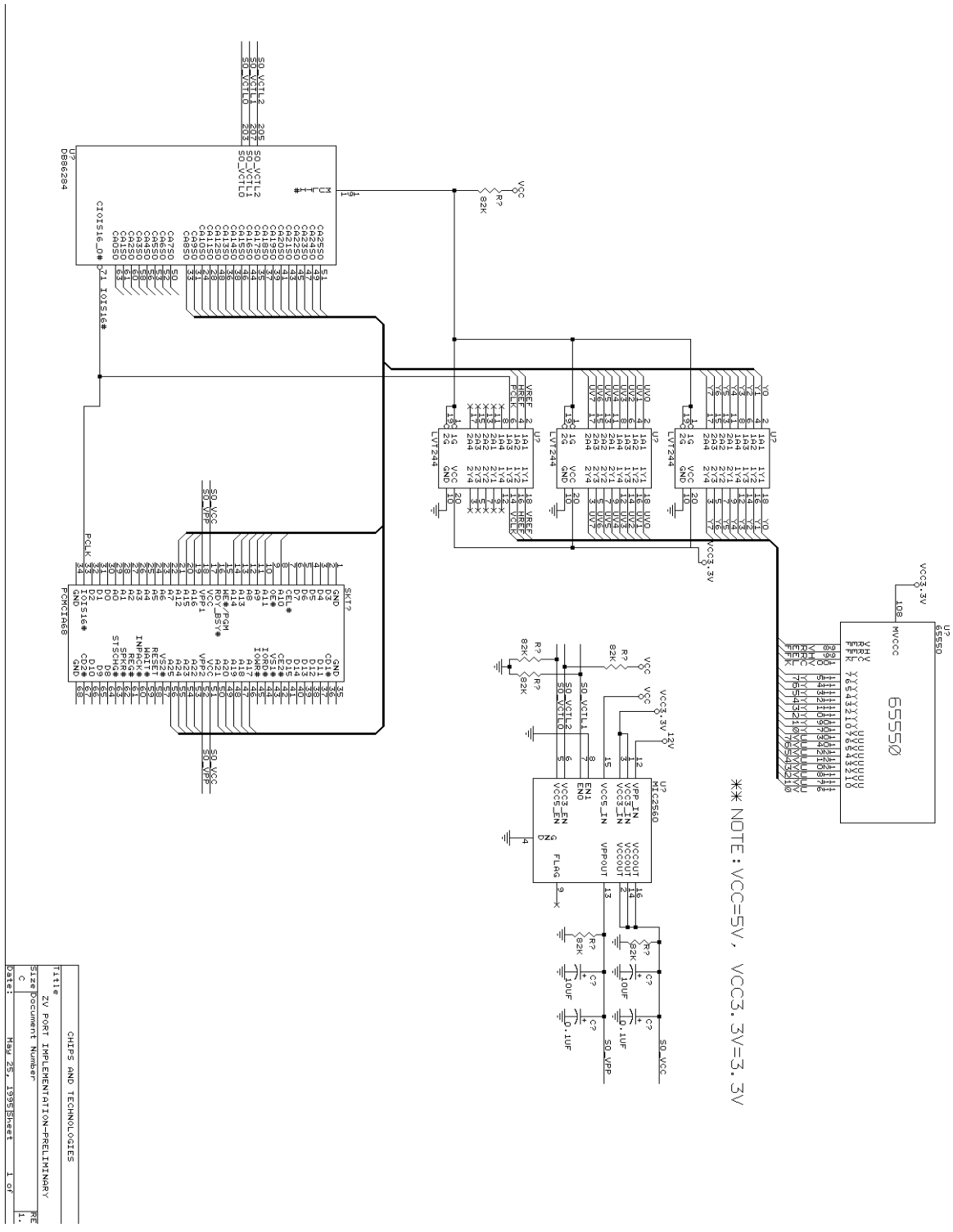
MR17: Acquisition Vertical Scale 7-0

MR18: Acquisition Capture Framecount 7-0

Schematic Example

In 65550, the higher 8 bits of panel interface (P16-P23) pins share the same voltage pin (pin 108-MVCCC) with the video capture port. The example ZV port system schematic shows the 65550 video capture port operating at 3.3V. This is OK as long as a 16-bit panel is used or if a 18/24bit-3.3V panel is used. In other words, if we are using a panel that has more than 16 data bits and the panel interface is 5V, then the video capture port must also be 5V.

Note: PCMCIA ZV port could operate at either 5V or 3.3V.


** NOTE: VCC=5V, VCC3.3V=3.3V
65550
MIC2560
LVT244
PCMCIA68
DB86204
ZV PORT IMPLEMENTATION-PRELIMINARY
CHIPS AND TECHNOLOGIES

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