THE CMOS/NANO INTERFACE FROM A CIRCUITS PERSPECTIVE

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Abstract—We consider a circuit paradigm that combines conventional silicon microelectronics with emerging self-assembled nanoelectronics. Peripheral CMOS circuitry is used to drive the input signals and restore the output signals of nanoscale crossbar structures. We address a number of issues dealing with interfacing CMOS and nanoelectronics. Furthermore, we consider important metrics, such as, delay, area, and energy for a full-adder implemented in the mixed circuit paradigm.

I. Introduction

The past few years have put forth remarkable demonstrations of novel nanoscale and molecular devices assembled into small circuits [1]. In addition, rapid advancements in conventional silicon electronics have spawned predictions of an accelerated path towards the silicon "brick wall" [2]. When considered separately, conventional silicon electronics and nanoelectronics present different views for the future of integrated circuits. Silicon has a proven track record and has already revolutionized our society, but it's ability to continue upon Moore's Law will eventually cease. On the other hand, nanoscale and molecular circuits have not yet been assembled into complex systems, yet they may hold the potential for reaching new levels of computation.

However, rather than considering a future based on either silicon or nanoelectronics, we believe hybrid solutions composed of both technologies will be the key for achieving new levels of performance, power, and density [3]. Although, the maturity of nanoscale and molecular circuits has not yet reached the VLSI level of fabrication, we are able to explore nanoscale circuits via simulation.

II. A CMOS/nano Circuit Paradigm

Developing an integrated circuit composed of conventional silicon electronics and novel nanoelectronics will encounter a variety of issues. Fabrication challenges for achieving acceptable yields will no doubt be numerous. However, in this paper we address some of the circuit design issues that arise.

A. Crossbar-Based Nanoelectronics

As conventional silicon devices push the 100nm barrier, traditional conceptions of nanoelectronics begin to blur. Therefore, we narrow our definition of nanoelectronics in this paper to nanoscale technologies that employ a "bottom-up" fabrication approach, such as self-assembly. We will refer to these technologies as *nano*. In turn, we will use the term *CMOS* refer to conventional solid-state technologies that rely on a "top-down" fabrication process, such as lithography. The key distinctions between these two fundamentally different fabrication approaches are the attainable features sizes and the freedom in determining arbitrary patterns. While a bottom-up process should allow smaller feature sizes, the resulting structures will typically be restricted to regular or periodic patterns. On the hand, top-down processes will be limited to larger feature sizes [4], but can realize arbitrary patterns. Thus, we believe the challenge of optimal CMOS/nano integration will be based on balancing the appropriate mixtures of smaller regular circuits (nano) and larger (CMOS) arbitrary circuits.

The most commonly targeted regular structure for self-assembled nanoelectronics is a crossbar. Fig. 1 shows a typical nanoscale crossbar structure that consists of a lower plane of parallel nanowires crossed perpendicularly by an upper plane of nanowires. A bistable junction exists between the wire crossings. The bistable junctions can be electrically altered to switch between a low resistance state (on-state) and a high resistance state (off-state). Typically the junction also has a diode-like behavior that allows currents flow under forward bias, but inhibits reverse bias current. This crossbar structure is a target for a variety physical implementations, such as, self-assembled nanowires, nanotubes, and nanoimprinted wires. Likewise, MRAM also consists conceptually of a similar crossbar structure with hysteretic junctions.

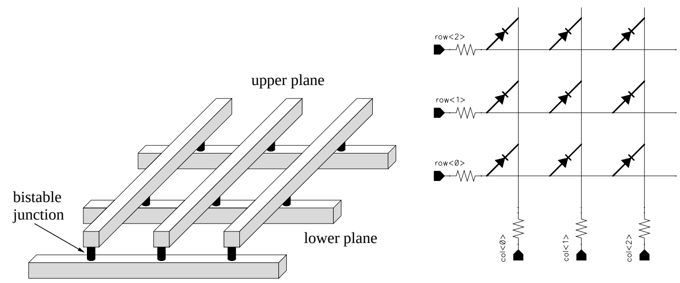


Fig. 1. A typical nanoscale crossbar structure consists of two planes of crossed nanowires with bistable devices at the junctions.

In particular, Hewlett-Packard and UCLA have pioneered the crossbar for molecular electronics [5], [6], [7], [8], [9]. Harvard has also demonstrated nanowire circuits that could be assembled in crossbar structures [10]. The promise of crossbar-based nanoelectronics has spawned a number of architectural ideas [11], [12], [13]. These works have motivated us to study circuit design issues for crossbars [3], [14].

B. The CMOS/nano Interface

In this paper, we consider interaction between on-chip CMOS circuits and nanoscale crossbar circuits. Unlike conventional CMOS, the nanoscale crossbars we consider do not have a fundamental dependency on the substrate, since the active devices are formed between the wire junctions. Thus, as in [3], we adopt the paradigm where the nano circuitry is fabricated on top of a conventional CMOS IC.

The physical properties of the CMOS/nano interface creates a number of fabrication challenges. However, there are higher-level issues when considering the CMOS/nano interface as well. Previous nano interface suggestions include nano decoder designs that are stochastic [7] or require nanoscale patterning resolution [13]. These CMOS/nano interface designs attempt to combine the following two goals:

Pitch Reduction - Communicating signals from the wire pitch in the CMOS technology, i.e., the microwire pitch (P_{micro}), to the nanoscale pitch in the nano crossbar, i.e., the nanowire pitch (P_{nano}).

Decoding - The ability to address a large address space in the nano crossbar with a smaller number of CMOS wires.

While we believe both pitch reduction and decoding are necessary, a solution we briefly outlined in [3] decouples the two goals. This approach relies on alignment precision for pitch reduction and a decoder programmed into the crossbar. As shown in Fig. 2, this approach begins

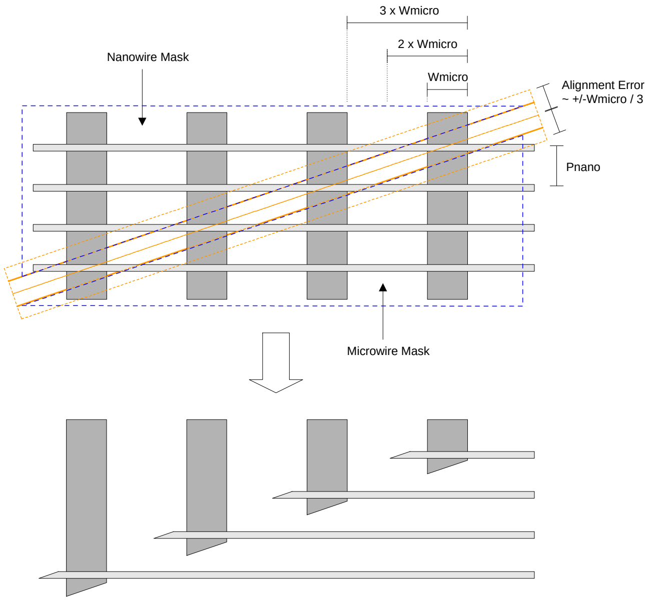


Fig. 2. Pitch reduction can be achieved by employing an interface scheme that relies on alignment accuracy.

with parallel nanowires perpendicularly overlapping an equal number of parallel microwires. Two masks are then used to remove the portions of the nanowires and microwires along a diagonal. This process assumes that the nanowires and microwires can be etched separately. The reliance on nanoscale pattern resolution is shifted to mask alignment precision. Using the rule of thumb that alignment will be equal to approximately one-third of the line width, this approach should be able reduce P_{nano} to at least the microwire line width (W_{micro}), as depicted in Fig. 2. Additional mask alignment accuracy as well as a number of other variations on this scheme should allow P_{nano} to be even smaller.

We can create nanowire crossbars by employing two or more of the interface structures described above, as shown in Fig. 3. We can then program the crossbar junctions by addressing individual crosspoints with the vertical programming microwires (connected to the horizontal nanowires) and horizontal address and data wires (connected to vertical nanowires). This scheme provides a mechanism to program a decoder into the crossbar. The decoder addresses a second crossbar we will refer to as the data array.

The decoder and data array pair can be used for logic or memory. The decoder is equivalent to a plane of AND gates, while the data array is essentially a plane of OR gates. Thus, two-level logic representations can be easily mapped to the crossbar. Fig. 4 shows a schematic of a full-adder realized in a crossbar along with the truth table.

Memory can also be implemented in these structures. However, memory requires the ability to program the data array via the decoder. Thus, to avoid inadvertently programming the decoder when writing to the data array, it may be necessary for the decoder to consist of junctions that are programmed at higher voltages than the data array.

To further reduce the area overhead associated with the CMOS/nano interface structure, it may also be desirable for multiple decoder and data array pairs to share the horizontal nanowires during the initial crossbar programming. This can be accomplished via a structure shown in Fig. 3. A method of post progamming isolation can then be used to allow each decoder and data array pair to function independently.

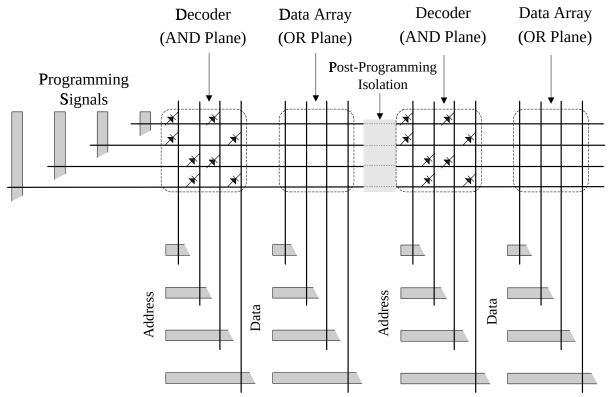


Fig. 3. A platform for logic and memory can be assembled by combining a number of diagonal interface structures.

Cin	A	B	Sum	Cout
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	0
0	1	1	0	1
0	1	0	1	0
0	0	1	1	0
0	0	0	0	0

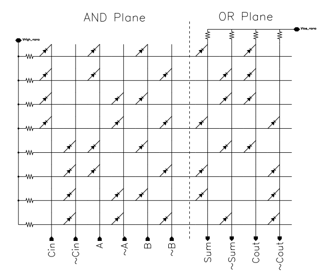


Fig. 4. The truth table for a full-adder and the corresponding mapping to a nano crossbar technology employing bistable diode junctions.

C. *CMOS Interface Circuitry*

Although the nano crossbar circuits hold the potential for high device densities, there are a number of inherent characteristics that pose problems for this technology alone. One of the most significant is the lack of signal gain in a diode-resistor circuit paradigm. Thus, signals on the crossbar must be periodically restored to the appropriate logic levels. In addition, the crossbar suffers from an inability to implement analog circuitry, a lack of an inversion function, and difficulty in implementing sequential logic. We suggested mixing nano crossbar circuits and CMOS on the same chip to achieve optimal device densities, performance, and power in [3]. In this paper we expand upon that notion by considering CMOS circuitry that can drive the nano crossbar inputs and sense the outputs. Fig. 5 shows a schematic of the mixed circuit. We have found that to meet certain design goals it may be advantageous to drive the nano crossbar with a different signal swing than the CMOS operating voltage levels. Thus, we use CMOS level shifters to drive the crossbar input lines. Furthermore, sense amplfiers are needed to restore the crossbar output signal to CMOS voltage levels. We use standard CMOS circuits for the level shifters and sense amplifiers, as shown in Fig. 6 a) and Fig. 6 b), respectively.

III. Circuit Simulation Results

For simulation we use the 70nm CMOS Predictive Technology Models (PTM) [15]. At the nano crossbar junctions we use models of the rotaxane molecules as described in [5] and [6]. The crossbar junctions are modeled with the Universal Device Model (UDM) [16] and implemented in Verilog-A. Our simulations use the Spectre circuit simulator from Cadence. Two additional system parameters of high importance are the contact resistance between the microwires and the nanowires

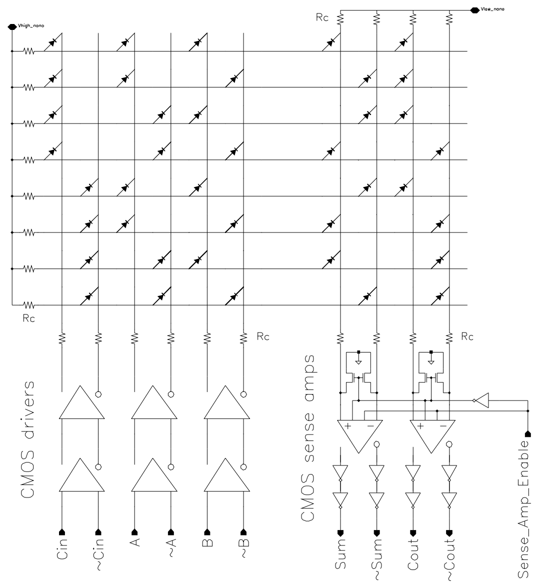
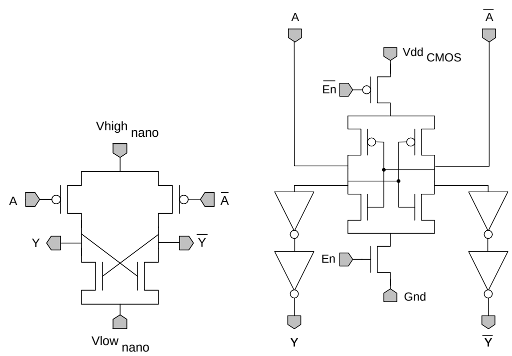


Fig. 5. The system we consider involves CMOS level shifters to drive the nano crossbar and CMOS sense amplifiers to restore the crossbar output to CMOS voltage levels.



a) b)

Fig. 6. We use standard CMOS circuits for the CMOS interface, a) level shifters driving the nano crossbar inputs, b) cross-coupled inverter latches to sense the outputs.

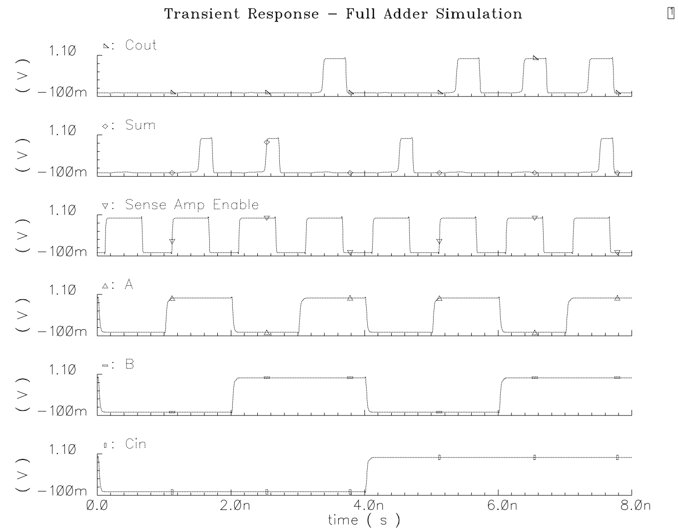


Fig. 7. Simulation waveforms for the nano crossbar and peripheral CMOS show the full-adder crossbar functioning correctly.

Performance	
Delay	491 ps
Cycletime	1 ns
Area	
Nano Crossbar	3 μm^2
Drivers	30 μm^2
Sense Amps	40 μm^2
Static Power	
Nano Crossbar	549 nW
Drivers	1.01 μW
Sense Amps	67.71 μW
Average Energy / Cycle	
Nano Crossbar	5.78e-16 J
Drivers	4.73e-14 J
Sense Amps	6.77e-14 J
Energy-Delay Product	5.67e-23 J-S

TABLE I

SIMULATED FIGURES OF MERIT FOR THE CROSSBAR FULL-ADDER.

(R_c) as well as the junction capacitance between the nanowires in the crossbar (C_j). The value of R_c is particularly important for the system we consider because it acts as the pull-up resistor for the AND plane and the pull-down resistor for OR plane. Likewise, the value of C_j is important because it determines the amount of capacitance that needs charged/discarged during switching. We set R_c to 1MΩ and C_j to 1aF, which is consistent with values from [8]. We assume the wire resistance of the nanowires, capacitance between the nanowires and substrate, and crosstalk capacitance between parallel wires are all negligible.

We use a 1 volt supply (Vdd_{CMOS}) for the 70nm CMOS circuitry; however, we have found that driving the nano crossbar with a 1 volt ($Vhigh_{nano}$) to -0.25 volt ($Vlow_{nano}$) signal swing provides a reasonable balance between performance and power consumption. Furthermore, we use 3 volts and -1.5 volts for the AND plane supply and OR plane supply of the crossbar, respectively. Finally, we use a differential sensing scheme that requires both the output signal and its complement to switch the sense amp. Despite the very small output voltage changes caused by the high resistance of the diode junction in the on-state in comparison to the contact resistance, the differential amplifiers are able to deterimine the correct output values. The simulated waveforms are shown in Fig. 7. Table I shows other figures of merits for the nano crossbar full-adder and peripheral CMOS.

Although the nano crossbar full-adder and peripheral CMOS we have simulated would be slower, larger, and consume more power in comparison to a full-adder implemented in 70nm CMOS, there are still a number of reasons to pursue mixed CMOS/nano circuits in the paradigm we have described above. More complex CMOS/nano systems will most likely target networks of crossbars, which may provide opportunities for reducing the amount of CMOS circuitry. Secondly, only about 0.5% of the average energy in Table I is consumed by the nano crossbar, while the rest is consumed by the peripheral CMOS. Further optimization of the peripheral CMOS may achieve additional reductions in energy, delay, and area.

In terms of area, we assume the nanowire pitch to be 70nm. To achieve the 70nm nanowire pitch, we estimate the microwire pitch to be 210nm. Table I shows our area estimates for the nano crossbar, which includes the diagonal interface structures and the crossbar itself. Area estimates for all the drivers and the sense amplifiers are also shown. Since the nano crossbar is on top of the peripheral CMOS, the total planar area will be determined only by nano crossbar area or the peripheral CMOS area, depending on which is greater. It is clear that the CMOS peripheral circuitry dominates the total area, while the nano crossbar occupies less than 4% of the total area. In comparison with a 70nm process standard library full-adder cell, we estimate the overall mixed CMOS/nano full-adder to be over twice the size of the library cell. However, considering only the nano crossbar and interface structures, the area would be only 11% of the full-adder library cell. From this we see that to take advantage of the small nano crossbar area, we need to reduce the amount of peripheral CMOS circuitry. A smaller amount of CMOS peripheral circuitry will also reduce energy. New nanoscale devices that can achieve signal gain and more complex crossbar structures are two possiblities for reducing the amount of CMOS peripherial circuitry.

Improving the present characteristics of the crossbar, such as, increasing the on-state current through the junctions and reducing the contact resistance, will enhance the performance of the crossbar. This would be particularly beneficial in the system we consider in this paper. Seeing that the resistance of the diode junction in the on-state is very large in comparison to the contact resistance, the output signals are inherently hampered.

However, entirely new devices will create new circuit paradigms. For example, devices that can provide gain without leaving the nano crossbar will allow extended levels of logic before interfacing to CMOS and allow a reduction in the amount peripheral CMOS. More elaborate crossbar structures may also make the CMOS/nano paradigm more advantageous. The addition of a third plane of parallel wires that cross the output nanowires provides an opportunity for a column decoder. Fig. 8 shows a crossbar system that allows multiple columns to share a sense amplifier. Likewise, this scheme allows parallel access to multiple data arrays, which reduces the number of drivers. Vertically stacking three or more nanowire planes may also allow additional density.

IV. Conclusion

While self-assembled nanoelectronics are still at an early stage of development, it is not too early to evaluate the potentials of these technologies. In this paper, we considered a crossbar-based nanoscale paradigm with peripheral CMOS circuitry. The nano crossbar paradigm contains inherent properties that will be advantageous for future electronics systems. However, for the paradigm we have considered here, it is clear that the overhead of the CMOS peripheral circuitry will need to be reduced to take advantage of the properties of the nanoscale technology. Further optimization of CMOS drivers and sense amplifiers specifically for nano integration may reduce the delay and energy of the mixed CMOS/nano circuits. In addition, new nanoscale devices that exhibit gain could allow extended computation without interfacing to CMOS, in turn reducing the amount of peripherial CMOS. Furthermore, more complex crossbar structures will allow more functionality to be shifted from the CMOS circuits onto the nano crossbar. Thus, there are a number of device, circuit, and architectural avenues that may lead to the raw density potentials inherent with self-assembled nanoelectronics.

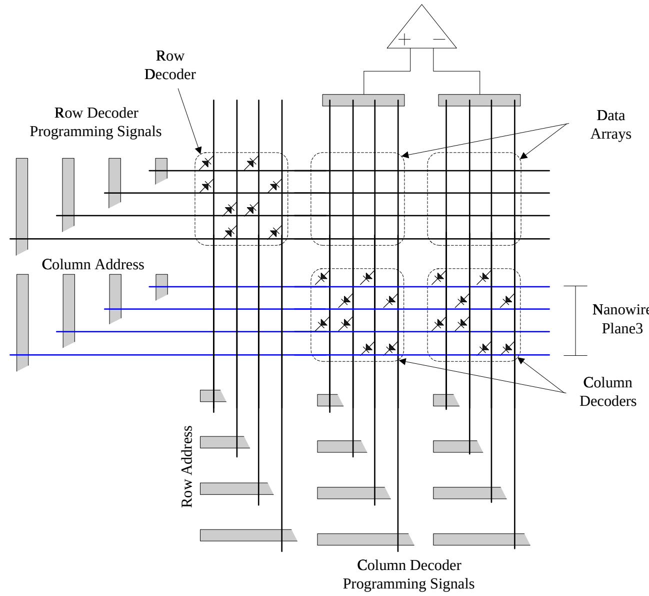


Fig. 8. The addition of a third plane of nanowires allows a column decoder to included in the nano crossbar structure.

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