# Michael Thaddeus Niemier

Assistant Professor

College of Computing
Georgia Institute of Technology
Atlanta, GA 30332-0280, USA

## Table of Contents

# EDUCATIONAL BACKGROUND

| Degree | Year | University | Field |
|---|---|---|---|
| **Ph.D.** | 2003 | University of Notre Dame, Notre Dame, IN., USA. | *Computer Engineering* |
| **M.S.** | 2000 | University of Notre Dame, Notre Dame, IN., USA. | *Computer Engineering* |
| **B.S.** | 1998 | University of Notre Dame, Notre Dame, IN., USA. | *Computer Engineering* |

# EMPLOYMENT HISTORY

| Title | Organization | Years |
|---|---|---|
| **Assistant Professor** | College of Computing Georgia Institute of Technology, Atlanta, GA., USA | *2003-present* |
| **Research Fellow** | Dr. Peter Kogge University of Notre Dame, Notre Dame, IN., USA | *1998-2003* |

# CURRENT FIELDS OF INTEREST

Computer architecture (for emergent, nanotechnologies), circuit design methodologies for emergent nanotechnologies, and defect tolerant and re-configurable computing.

**Goals:**

My research address a current obstacle between the individuals interested in designing systems of nano-scale devices, and the physical scientists who must actually build them. At present, there is much ongoing research concerning nano-scale devices geared toward computation; but most work is exactly that – device work. Only the simplest circuits and systems comprised of such devices – which are the desired end result – have been proposed, let alone simulated and built. Further, virtually all existing circuits and systems for any emergent device have been proposed by the device engineers themselves whose background lies in the physical sciences, not systems engineering. While physical science may be able to propose a functionally complete system, making one that is computationally interesting and efficient is aided by individuals with a systems background. Still, while a system designer can help generate some computationally interesting circuits, he or she almost assuredly does not possess all of the physical science knowledge that would assure such a system is feasible to implement. As most research with nano-scale devices is inherently interdisciplinary, collaborations between both groups is essential – which should help to create system designers who understand relevant physical science, and eventually realized computational systems in an accelerated time frame.

# I. TEACHING

## A. Courses Taught

| Quarter/Year | Course Number & Title | Number of Students | Comments |
|---|---|---|---|
| **Department of Computer Science and Engineering, University of Notre Dame.** | | | |
| Spring, 2002 | CSE 521 Graduate Computer Architecture | 20-25 | Lecture |
| Spring, 2003 | CSE 521 Graduate Computer Architecture | 20-25 | Lecture |
| **College of Computing, Georgia Institute of Technology.** | | | |
| Spring, 2004 | CS 2200 Systems and Networks | 50-60 | Lecture |

## B. Curriculum Development

**College of Computing, Georgia Institute of Technology, Atlanta, GA.**

**Nanocomputing Course (with Ralph Merkle):** Specific topic areas to be covered will focus on computational devices and include: modeling and simulation techniques, fundamental device physics, manufacturability, possible system architectures, and desired device characteristics for computationally interesting systems. Several course modules will also be developed for Georgia Tech's existing MSE 2001 - Principles and Applications of Engineering Materials in the College of Engineering (COE) - on the Structure and Properties of Nanomaterials. Analysis of the proposed COC course will be used to discern what courses would best form a specialization in nanotechnology in the COC (College of Computing). Proposed courses would be interdisciplinary, making it the first COC specialization to be so, and will specifically address the aforementioned "gap in understanding" from a systems perspective in COC's curriculum. Additionally, currently, the COE offers a certificate in nanotechnology, with approved courses currently coming from the MSE, CHEM, PHYS, and ECE disciplines. The proposed COC course would be added to this list allowing the certificate to cross college boundaries, and again addressing the above "gap in understanding" - but this time from a physical device perspective.

**High School Outreach:** Organizing demonstrations of nanotechnology, general computing, my research, etc. to be presented at Tech High School with physics teacher Alan Gravitt (also of Tech High School). This is also being done in conjunction with CEISMC.

## C. Individual Student Guidance

*Ramprasad Ravichandran:* Independent study (8803) concerning design rules and design methodologies for implementable QCA circuits and systems (Spring/Summer 2004); I will fund his research in the Fall of 2004.

*Shetu Shah:* Independent study (8803) concerning systolic architectures for systems of QCA cells, as well as DNA-based computation (Spring/Summer 2004); I will fund his research in the Fall of 2004 and also supervise a M.S. Thesis.

*Adam Johnson* Funding Adam as a research assistant to investigate counterflow pipeline processors for QCA (Spring/Summer 2004).

*Nick DePalma:* Supervising undergraduate Nick DePalma who will study and model defects in QCA circuits and systems.

*Mariam Mathew:* Supervising undergraduate Mariam Mathew who will investigate several computing applications based on silicon nanowires and carbon nanotubes. This work should lead to a paper comparing all of the most promising devices for nano-scale computation to see what tasks each can perform, how they perform, etc. (Mariam is actually an MSE student).

*Kamaram Munira:* Supervising undergraduate Kamaram Munira who will investigate several computing applications based on silicon nanowires and carbon nanotubes. This work should lead to a paper comparing all of the most promising devices for nano-scale computation to see what tasks each can perform, how they perform, etc.

**Post-Doctoral Fellows**

None.

**Ph.D. Students Supervised (in process as well as graduated)**

None.

**Ph.D. Special Problems students.**

None.

**M.S. Thesis Students supervised.**

I will supervise Shetu Shah's M.S. Thesis, starting in Fall, 2004.

**MS. Special Problems students.**

None.

**Undergraduate Research Students.**

None.

## D. Teaching Honors and Awards

1. None.

# II. RESEARCH AND CREATIVE SCHOLARSHIP

## A. Thesis

**M.S. Thesis**

Title: *"Designing Digital Systems in Quantum Cellular Automata"*
Date Completed: *March, 2000,*
Advisor: *Dr. Peter Kogge,*
University: *University of Notre Dame.*

**Ph.D. Thesis**

Title: *"The Effects of a New, Nanotechnology on the Design, Organization, and Architectures of Computing Systems"*
Date Completed: *September, 2003*,
Advisor: *Dr. Peter Kogge*,
University: *University of Notre Dame.*

## B. Published Journal Papers (refereed)

B.0.1 Niemier, M.T. and Kogge, P.M., "Problems in Designing with QCAs: Layout = Timing", In *International Journal of Circuit Theory and Applications*, 29: 49-62, 2001.

## C. Published Books and Parts of Books (Refereed)

### C.1. Chapters in Books

C.1.1 Lent, C.S., Snider, G.L., Bernstein, G., Porod, W., Orlov, A., Lieberman, M., Fehlner, T., Niemier, M.T., Kogge, P.M. "Quantum-Dot Cellular Automata." Chapter in *Electron Transport in Quantum Dots*, pp. 397-433, Johahtan P. Bird (ed.), Kluwer Academic Publishers, 2003.

C.1.2 Niemier, M.T., Kogge, P.M. "Origins of Design Rules for QCA" *Nano, Molecular, and Quantum Computing: Are We Ready for the Validation and Test Challenges*, Iris Bahar and Sandeep Shukla (Editors), to appear, Kluwer Press, 2004.

C.1.3 Nguyen, J., Ram, R. Lim, S.K., Niemier, M.T. "Origins of CAD tools for QCA Systems" *Nano, Molecular, and Quantum Computing: Are We Ready for the Validation and Test Challenges*, Iris Bahar and Sandeep Shukla (Editors), to appear, Kluwer Press, 2004.

## D. Edited Proceedings and Collections

D.0.1 None.

## E. Conference Presentations

### E.1. Invited Keynote Addresses

E.1.1 None

### E.2. Conference Presentations with Proceedings (refereed and archival)

*[Refereed publications in respected conferences, with extensive reviewing, and appearing in archival proceedings.]*

E.2.1 Antonelli, D.A., Dysart, T.J., Chen, D.Z., Hu X.S., Kahng, A.B., Kogge, P.M., Murphy, R.C., Niemier, M.T., "Quantum-Dot Cellular Automata (QCA) Circuit Partitioning: Problem Modeling and Solutions", to appear in the Proceedings of the 41st Design Automation Conference, June 7-11, 2004, San Diego, CA.

E.2.2 Niemier, M.T. and Kogge, P.M. "Logic in Wire: Using Quantum Dots to Implement a Microprocessor", , In *Proceedings of the 9th Great Lakes Symposium on VLSI*, pp. 122-125, IEEE Computer Society Press, Ann Arbor, MI, March 2-4, 1999.

E.2.3 Niemier, M.T. and Kogge, P.M. "Design Complex Logic Systems with QCA Devices", , In *Proceedings of the International Conference of Electronics, Circuits, and Systems*, IEEE Computer Society Press, Larnaca, Cyprus, September 1999.

E.2.4 Niemier, M.T., Kontz, M.J., and Kogge, P.M. "A Design of and Design Tools for a Novel Quantum Dot Based Microprocessor", , In *Proceedings of the 37th Design Automation Conference*, pp. 227-232, Association for Computer Machinery (ACM) Press, Los Angeles, CA, June 2000.

E.2.5 Niemier, M.T. and Kogge, P.M. "Exploring and Exploiting Wire-Level Pipelining in Emerging Technologies", , In *Proceedings of the 28th International Symposium of Computer Architecture*, pp. 166-177, IEEE Computer Society Press, Goteburg, Sweden, July 2001.

E.2.6 Niemier, M.T. and Kogge, P.M. "The '4-Diamond' Circuit - A Minimally Complex Nano-scale Computational Building Block in QCA", , In *Proceedings of the IEEE Computer Society Symposium on VLSI*, pp. 3-10, IEEE Computer Society Press, Lafayette, LA, February 2004.

E.2.7 Ravichandran, R., Ladiwala, N., Nguyen, J., Niemier, M., Lim, S.K. "Automatic Cell Placement for Quantum-dot Cellular Automata", , To Appear In *Proceedings of the 14th Great Lakes Symposium on VLSI*, Boston, MA, April 2004.

### E.3. Conference Presentations with Proceedings (refereed)

*[Publication (as a full paper, a short paper or a technical note) in peer refereed conference/workshop proceedings.]*

E.3.1 Niemier, M.T. and Kogge, P.M. "Logic-in-Wire: Using Quantum Dots to Implement Really Dense Processing Logic", In *Proceedings of the Third Petaflops Workshop held in conjunction with Fronteirs of Massively Parallel Processing*, Annaopolis, MD, February 1999.

E.3.2 Niemier, M.T., Rodrigues, A.F., Kogge, P.M. "A Potentially Implementable FPGA for Quantum Dot Cellular Automata", In *1st Workshop on Non-Silicon Computation (NSC-1), held in conjunction with the 8th International Symposium on High Performance Computer Architecture (HPCA-8)*, Boston, MA, February 2002.

E.3.3 Niemier, M.T. and Kogge, P.M. "Teaching Students Computer Architecture for New Nanotechnologies", , In *Workshop on Computer Architecture Education (WCAE), held in conjunction with the 29th International Symposium of Computer Architecture (ISCA)*, Anchorage, AK, May 2002.

### E.4. Conference Presentations without Proceedings (abstract refereed)

E.4.1 Niemier, M.T. and Kogge, P.M. "Designing a Microprocessor Using Quantum Cellular Automata (QCA)", At *6th MEL-ARI Review*, Duisburg, Germany, July 1999.

E.4.2 Niemier, M.T. and Kogge, P.M. "Quantum Cellular Automata", At *Nanotech*, Houston, TX, September 2000.

### E.5. Conference Presentations: Tutorial and Courses

E.5.1 None.

## F. Other

### F.1. Submitted Journal Papers

F.1.1 Niemier, M.T. and Ravichandran, R. "A Design Methodology for Computationally Interesting *and* Buildable QCA Circuits and Systems", To be submitted to *IEEE Transactions on Nanotechnology* or *IEEE Transactions on Circuits Systems* 7/04- 8/04.

F.1.2 Niemier, M.T., Hu, S., and Chen, D. "Challenges and Opportunities for Success in QCA CAD", To be submitted to *IEEE Transactions on CAD* or *IEEE Transactions on Nanotechnology* or *ACM Transactions on Design Automation* or *The New ACM Nano-Journal* 7/04 - 8/04.

F.1.3 Niemier, M.T. and Kogge, P.M. "Design FPGAs in QCA", To be submitted to *IEEE Transactions on Nanotechnology* 7/04 - 9/04.

F.1.4 Niemier, M.T. and Kogge, P.M. "Teaching Students how to Design given the new Paradigms of Nano-scale Devices: Evolving vs. Adapting", To be submitted to *IEEE Transactions on Education* 7/04 - 9/04.

### F.2. Submitted Conference Papers

F.2.1 Niemier, M.T. and Kogge P.M. "The Foundation for Design Rules in the Quantum-Dot Cellular Automata (QCA)", To be submitted to *T.B.D.* 6/04 - 7/04.

### F.3. Technical Reports

F.3.1 None.

### F.4. Software

F.4.1 None.

### F.5. Published Papers (non-refereed)

F.5.1 None.

## G. Research Proposals and Grants (Principal Investigator)

### 1. Approved and Funded

G.1.1 Automatic Placement Algorithms for Quantum-dot Cellular Automata. NSF(NER) M.T. Niemier and S.K. Lim. $129,734 for 1 year. Submitted October 2003.

### 2. Pending

G.2.1 Toward Molecular Circuit Boards: Circuit Design, Synthesis, and Defects in Self-Assembling DNA Structures. NSF(ECS) M.T. Niemier and M. Lieberman. $538,898 for 3 years. Submitted February 2004.

G.2.2 EMT: Using CAD to Advance Realizable Computing Capabilities in the Quantum-dot Cellular Automata. NSF(EMT) M.T. Niemier and Sung Kyu Lim. $375,360 for 3 years. Submitted March 2004.

G.2.3 Modeling an adiabatic clock structure for QCA circuits and systems with SPICE. Semiconductor Research Corporation X. Sharon Hu, Peter M. Kogge, and M.T. Niemier. $84,500 for 1 year. Submitted June 2004.

G.2.4 A Multi-threaded, Distributed Simulator for Physical Systems of QCA Cells. Nanoscience Nanoengineering Research Program (NNRP) at Georgia Tech. Richard Fujimoto and M.T. Niemier. $50,000 for 1 year. To be submitted July 9, 2004.

G.2.5 A Design Methodology for QCA. NSF(CAREER) M.T. Niemier. Approximately $400,000 for 4 years. To be submitted July 21, 2004.

### 3. Not Funded

G.3.1 Computational Nanotechnology: Coupling Nanomaterials and Design. NSF(NUE) M.T. Niemier, J. Hampikian, B. Klein, R. Merkle, and Z.L. Wang $100,000 for 2 years. Submitted November 2003. Will resubmit in 2004.

## H. Research Proposals and Grants (Contributor)

### 1. Approved and Funded

H.1.1 None.

### 2. Pending

H.2.1 NSF RI Proposal at the Georgia Institute of Technology (2003).

### 3. Not Funded

H.3.1 NSF NSEC: "The Development of Molecular Integrated Nanoelectronics (with the University of Notre Dame)." (2003).

## I. Research Honors and Awards

- National Science Foundation Fellowship (1999).
- Arthur J. Schmidtt Graduate Fellowship from the University of Notre Dame (1998).
- Third place in Design Automation Conference student design contest (2000).

# III. SERVICE

## A. Professional Activities

### A.1. Memberships and Activities in Professional Societies

- Member, Institute of Electrical and Electronics Engineers (IEEE).
  - IEEE Computer Society.
- Member, Eta Kappa Nu, Tau Beta Pi.

### A.2. Conference Committee Activities

1. Program Committee for 3rd Workshop on Non-silicon Computation in conjunction with International Symposium of Computer Architecture, 2004.
2. Program Committee for 2005 Design Automation and Test in Europe (DATE).
3. Organizing special session for International Conference on Circuit Design (ICCD), 2004.

## B. Awards

1. None.

## C. On-Campus Georgia Tech Committees

1. Member, Georgia Tech's College of Computing Faculty Recruiting Committee, 2003-2004.
2. Organizing a retreat within COC to discuss research efforts and collaborations in nanotechnology.

## D. Member of Ph.D. Examining Committees

**Ph.D. Examining Committee – Georgia Tech.**

1. None.

**Ph.D. Area Exam Committee – Georgia Tech.**

1. None.

## E. Consulting, Advisory, and Other External Appointments

- None.

# IV. NATIONAL AND INTERNATIONAL PROFESSIONAL RECOGNITION

## A. Invited Conference Session Chair

1. None.

### B. Editorial and Reviewer Work for Technical Journals and Publishers

1. IEEE Transactions on Nanotechnology.
2. IEEE Transactions on Parallel and Distributed Systems.
3. Third Workshop on Non-Silicon Computation.

### C. Patents

- None.

## V. OTHER CONTRIBUTIONS

### A. Seminar Presentations (Invited Papers and Talks at Meetings and Symposia)

1. None.

## VI. PERSONAL DATA


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|---|---|
| Born: | 24 May 1976, South Bend, IN USA. |
| Home Address: | 7106 Chastain Dr. NE<br>Atlanta, GA 30342. |
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