The future of nano-computing

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Intel Corporation

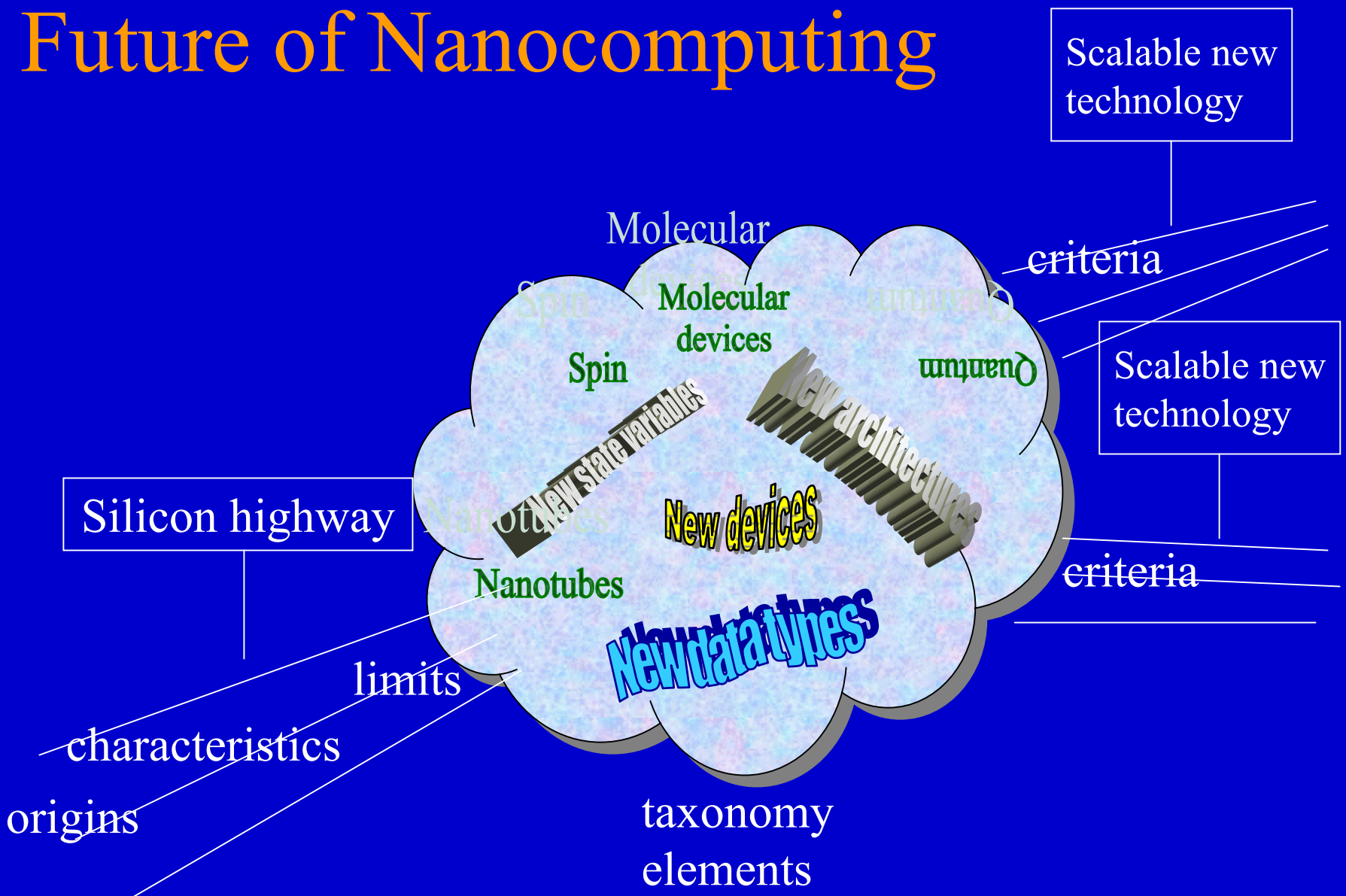
Presented to

International Engineering Consortium and

Electrical and Computer Engineering Department Heads

Jan. 27, 2003 San Jose, Ca

Future of Nanocomputing



Key messages

- CMOS scaling will continue for next 12 –15 years
- Alternative new technologies will emerge and begin to be integrated on CMOS by 2015
- Nanoscience research is needed to facilitate radical new scalable technologies beyond 2020

The future of nanocomputing

- Introduction
- Scaled CMOS
- Nano-computing, nano-technology and nano-science
- Radical new technologies
- Challenges
- Conclusions

The foundations of microelectronics

Government funded research in solid state physics in 1930's and 40's laid the foundation

Central Breakthroughs:

- Band structure concept
- Minute amounts of impurities control properties
- Advances in purification and high quality crystal growth of Si and Ge

Beginning about 1946, we began to utilize this knowledge base

Most basic semiconductor devices were demonstrated within 12 years

Bipolar transistor	**1948**
Field effect transistor	**1953**
LED	**1955**
Tunnel diode	**1957**
IC	**1959**
Laser	**1960**

The beauty of silicon

For four decades, the semiconductor industry has steadily reduced the unit cost of IC components by

1. Scaling device dimensions downward
2. Scaling wafer diameter upward

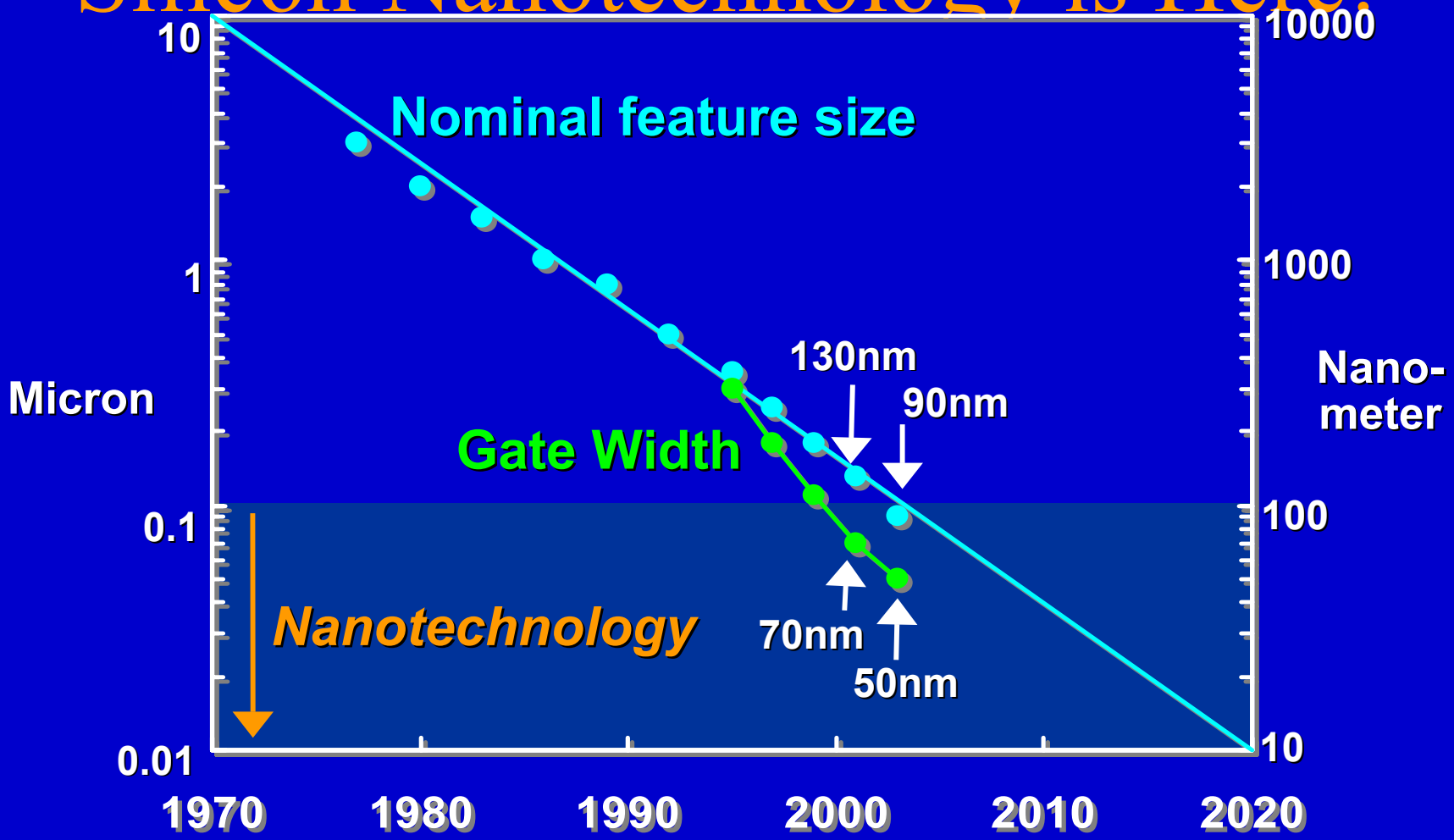
	1990	1995	2000
DRAMs	4 MB	64 MB	1 GB
Feature size	0.8 μm	0.35 μm	0.15 μm
Wafer diameter	6”	8”	12”
Cost per Megabit	$6.50	$3.14	$0.10

Brick Walls on the ITRS

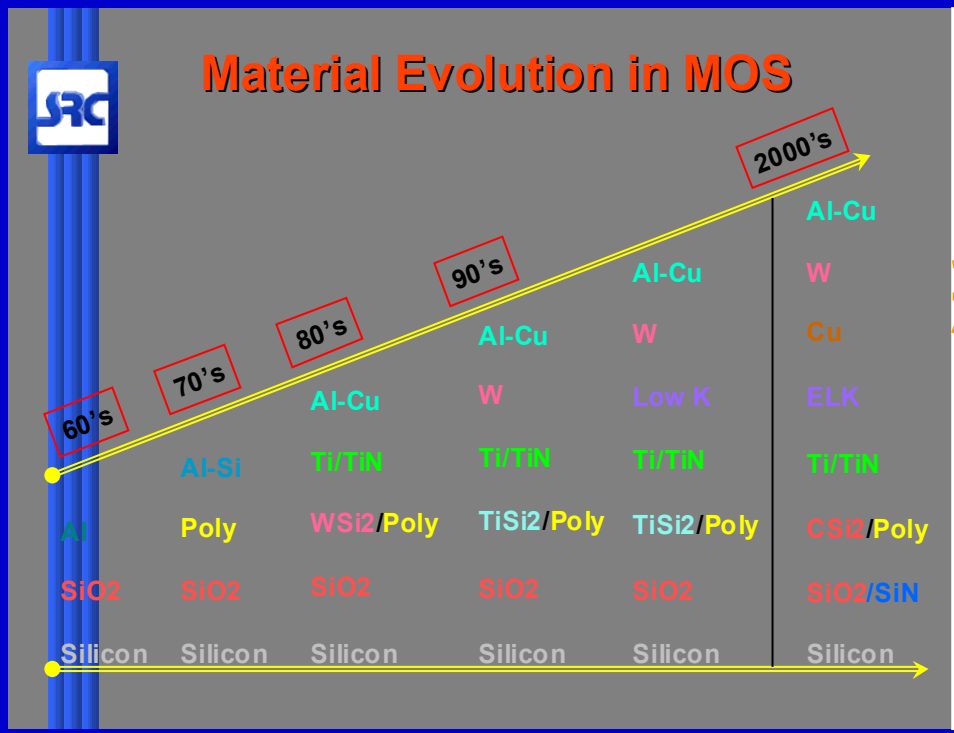
YEAR TECHNOLOGY NODE	1999 180 nm	2002 130 nm	2005 100 nm	2 70	2008 70 nm	2011 50 nm	2014 35 nm
On-chip local frequency (MHz)	1.25	2.10	3.50	6	6.00	10.00	13.50
Number of metal levels - Logic	6-7	7-8	8-9		9	9-10	10
Number of optional levels	0	2	2		3	4	4
Jmax (A/cm^2) - wire (at 105^{o}C)	5.8 E5	9.6 E5	1.4 E6	2.	2.1 E6	3.7 E6	4.6 E6
Local wiring pitch - DRAM non-contacted (nm)	360	260	200		140	100	70
Local wiring pitch - Logic (nm)	500	325	230		165	120	85
Local wiring AR-Logic (Cu)	1.4	1.5	1.7		1.9	2.1	2.2 - 2.3
Cu local dishing (nm)	18	14	11		9	7	5
Intermediate wiring pitch - Logic (nm)	560	405	285		210	145	110
Intermediate wiring h/w AR - Logic (Cu DD via/lin)	2.0/2.1	2.2/2.1	2.4/2.2	2.	2.5/2.3	2.7/2.4	2.9/2.5
Cu intermediate wiring dishing - 15 um wide wire (nm)	64	51	41		30	22	17
Dielectric erosion, intermediate wiring 50% density (nm)	64	51	41		0	0	0
Global wiring pitch - Logic (nm)	900	650	460		330	240	170
Global wiring h/w AR - Logic - Cu DD via/line (nm)	2.2/2.4	2.5/2.7	2.7/2.8	2.	2.8/2.9	2.9/3.0	3.0/3.1
Cu global wiring dishing, 15 um wide wire (nm)	116	95	76		55	38	20
Contact aspect ratio - DRAM, stacked cap	9.3	11.4	13		14.1	16.1	23.1
Conductor effective resistivity (uohm -cm)	2.2	2.2	2.2		1.8	< 1.8	< 1.8
Barrier/cladding thickness (nm)	17	13	10		0	0	0
Interlevel metal insulator effective dielectric constant (k) - Logic	4.0 - 3.5	3.5 - 2.7	2.2 - 1.6	1.4	1.4	<1.5	<1.5

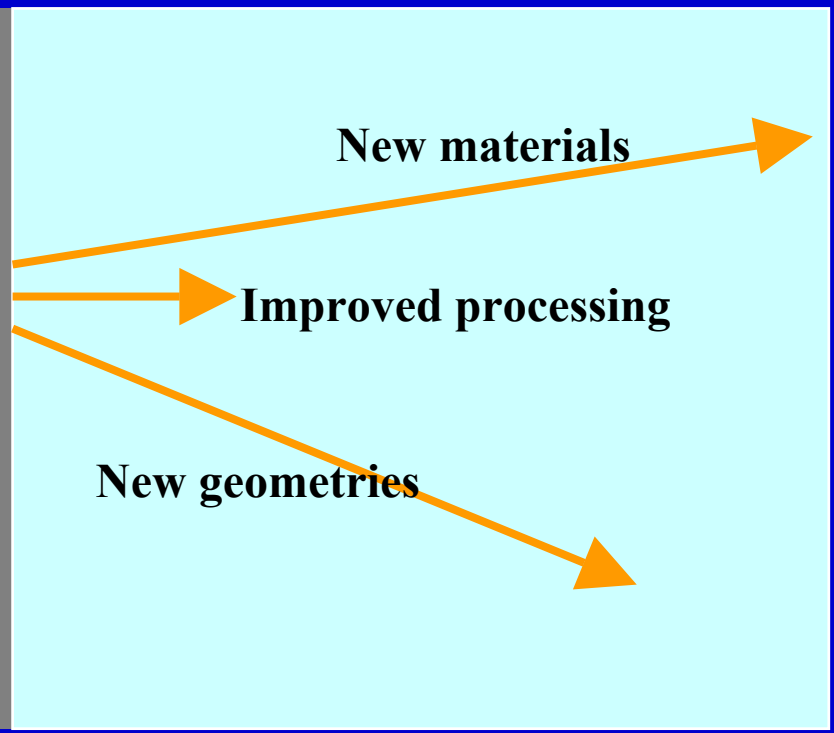
Solutions Exist
Solutions being pursued
No known solutions

Silicon Nanotechnology is Here!



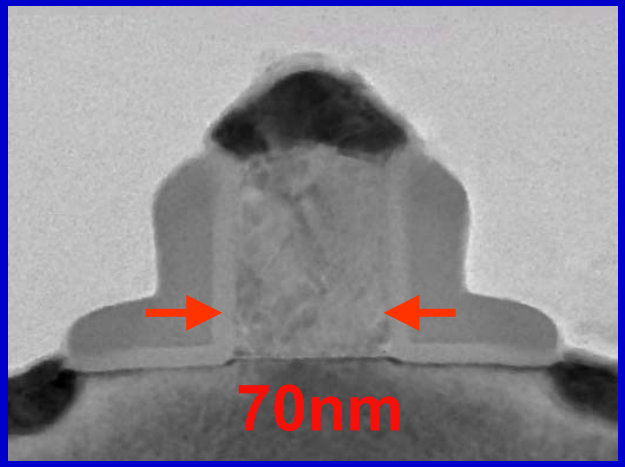
The ingredients of scaling





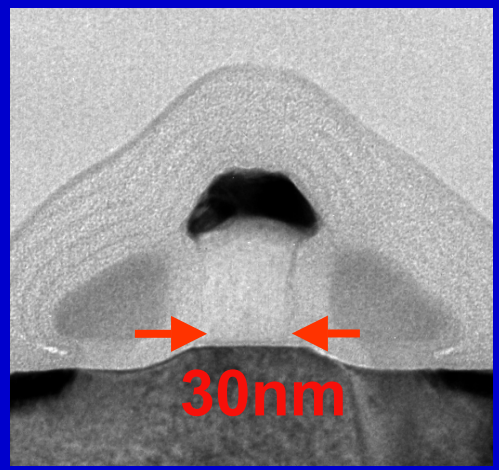
Scaling Will continue as long as
(δ cost) /(δ performance) < alternate technologies

Transistor Scaling

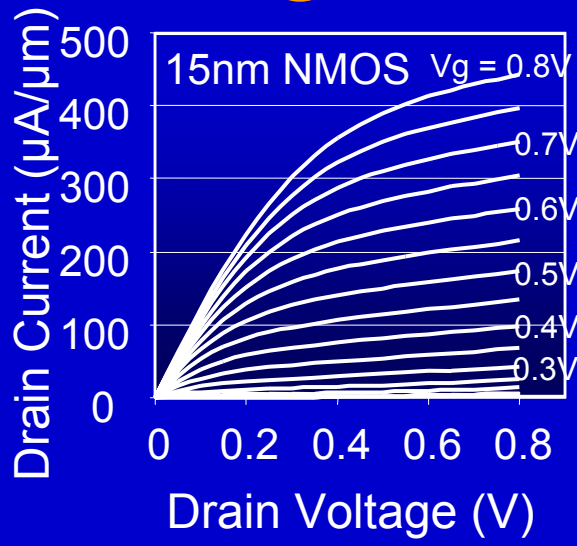


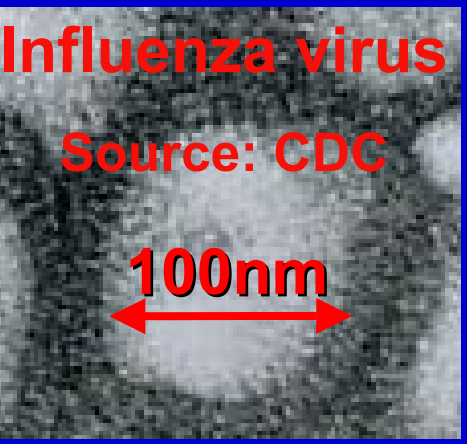
70nm transistor
for 0.13µm process
2001 production

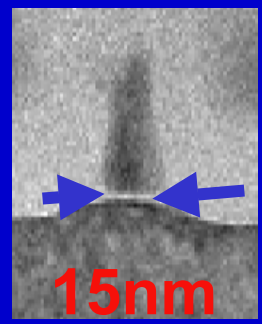
Demo: 2000



30nm transistor
Prototype







15nm transistor
prototype

Source:
Intel (IEDM, Dec 2001)

New Materials

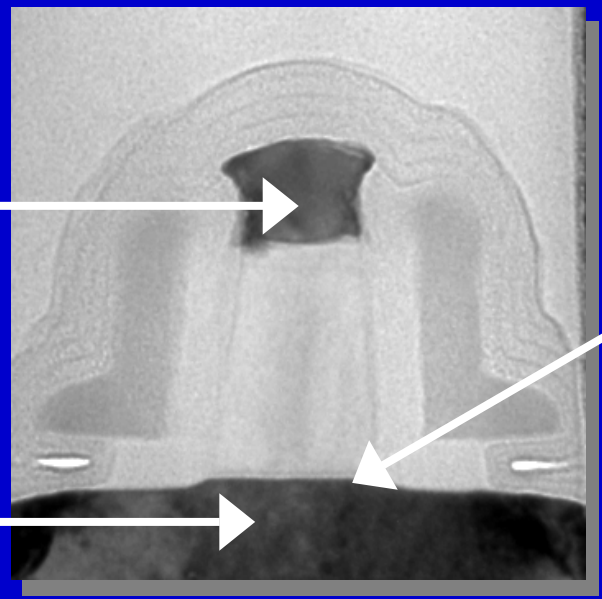
Changes Made

Gate

Silicide added

Channel

Strained silicon



Transistor

Future Options

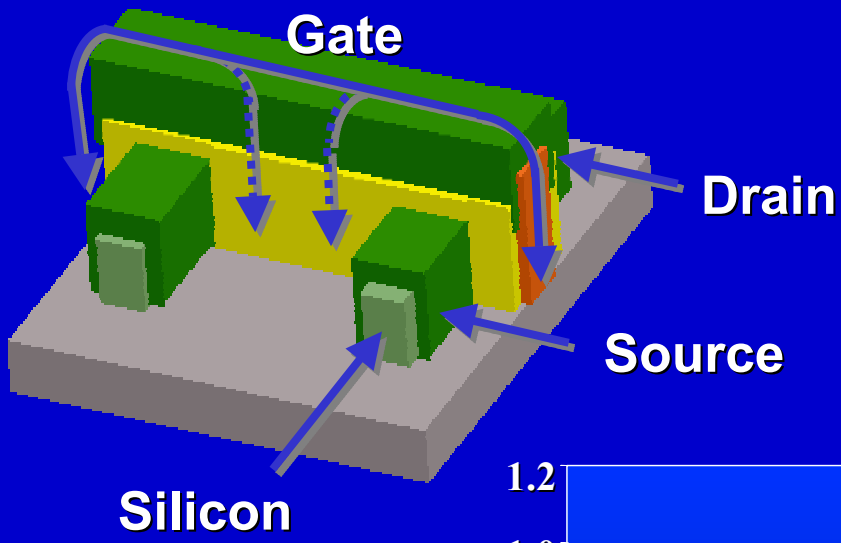
High-k gate dielectric

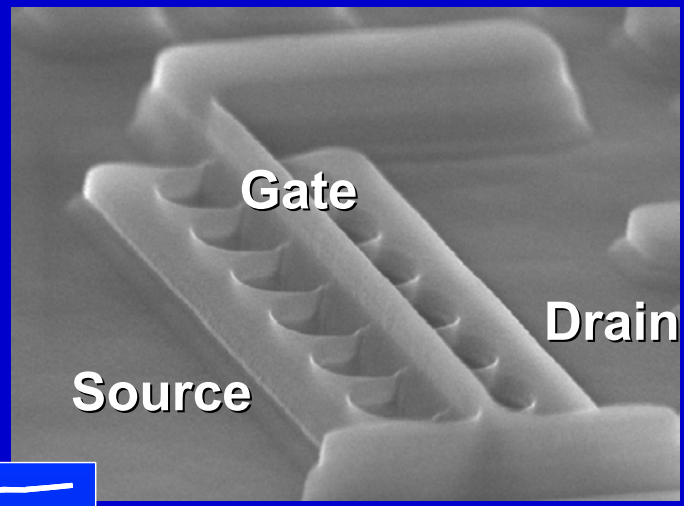
New transistor structure

Source: Intel

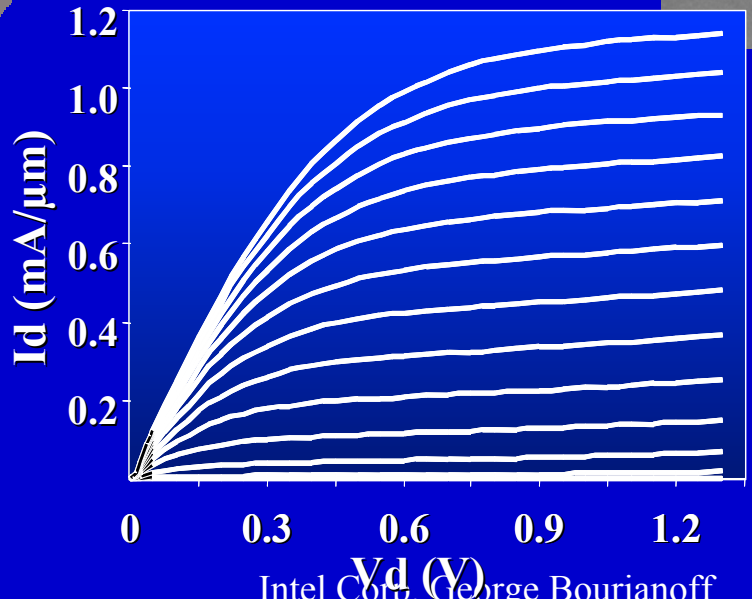
The problem: High Ioff current

New Geometries



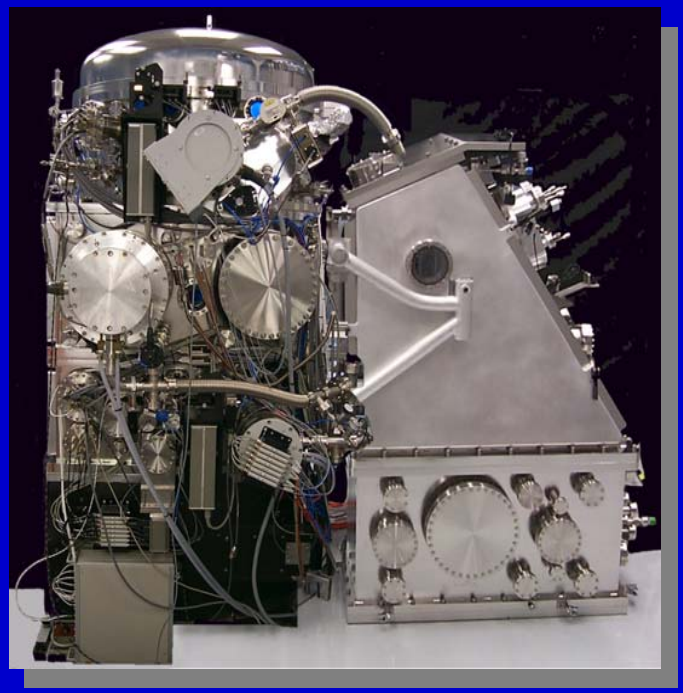


Source: Intel
(ISSDM, Sep 2002)

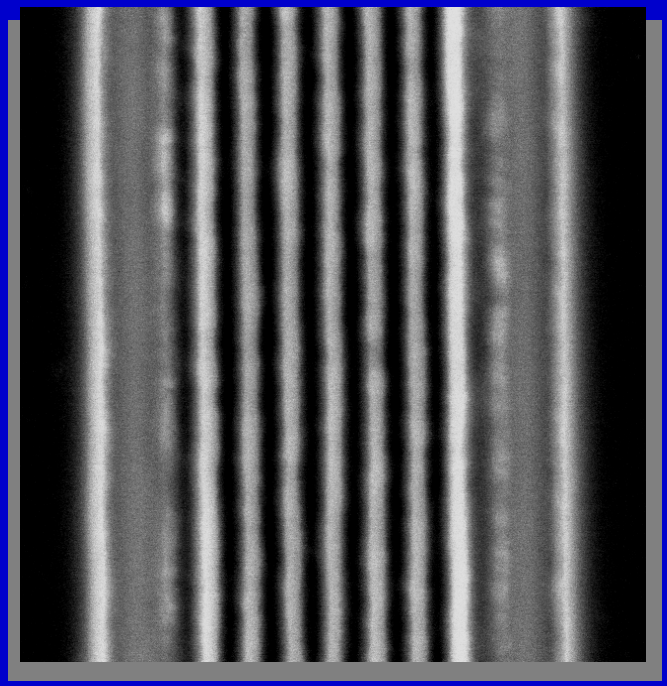


Source: Intel

Improved processing



EUV Lithography
Prototype Exposure Tool



50nm Lines Printed
with EUV Lithography

EUV lithography in commercialization phase
Cost effectiveness is key challenge

Source: Sandia

The limits of logic scaling

- For an *arbitrary* switching device made of of a single electron in a dual quantum well
  - Operating at room temperature
- It can be shown a power dissipation limit of 100 W/cm**2
- Will limit the operational frequency to ~100 GHz at length scales ~ 4 nm

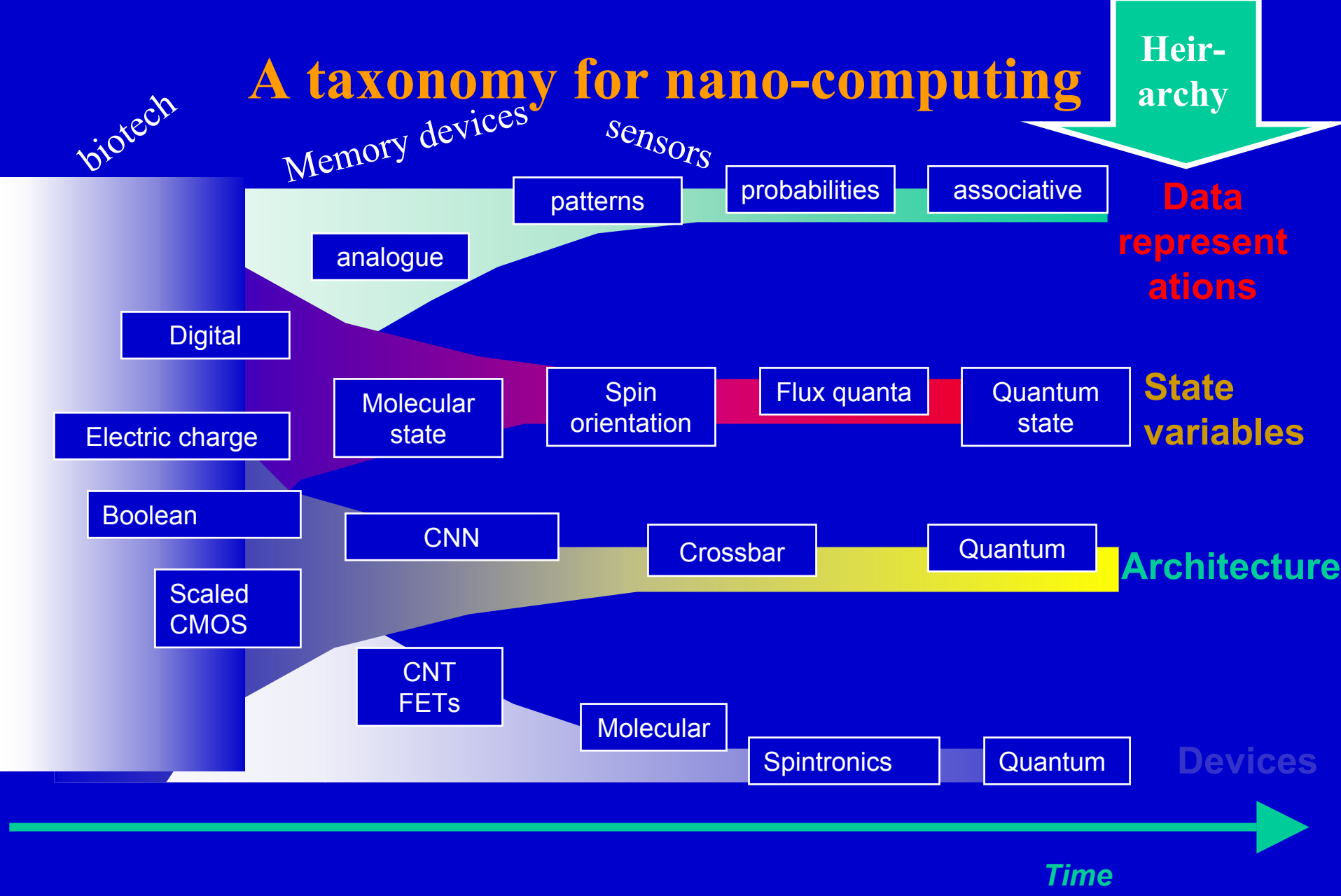
CMOS device circa 2016

- **Cost** **10^{-11} $/gate**
- **Size** **8 nm / device**
- **Speed** **0.2 ps /operation**
- **Energy** **10^{-18} J/operation**

The future of nanocomputing

- Introduction
- Scaled CMOS
- **Nano-computing, nano-technology and nano-science**
  - **A taxonomy**
  - New devices
  - New architectures
  - Alternative state variables
- Radical new technologies
- Challenges
- Conclusions

A taxonomy for nano-computing



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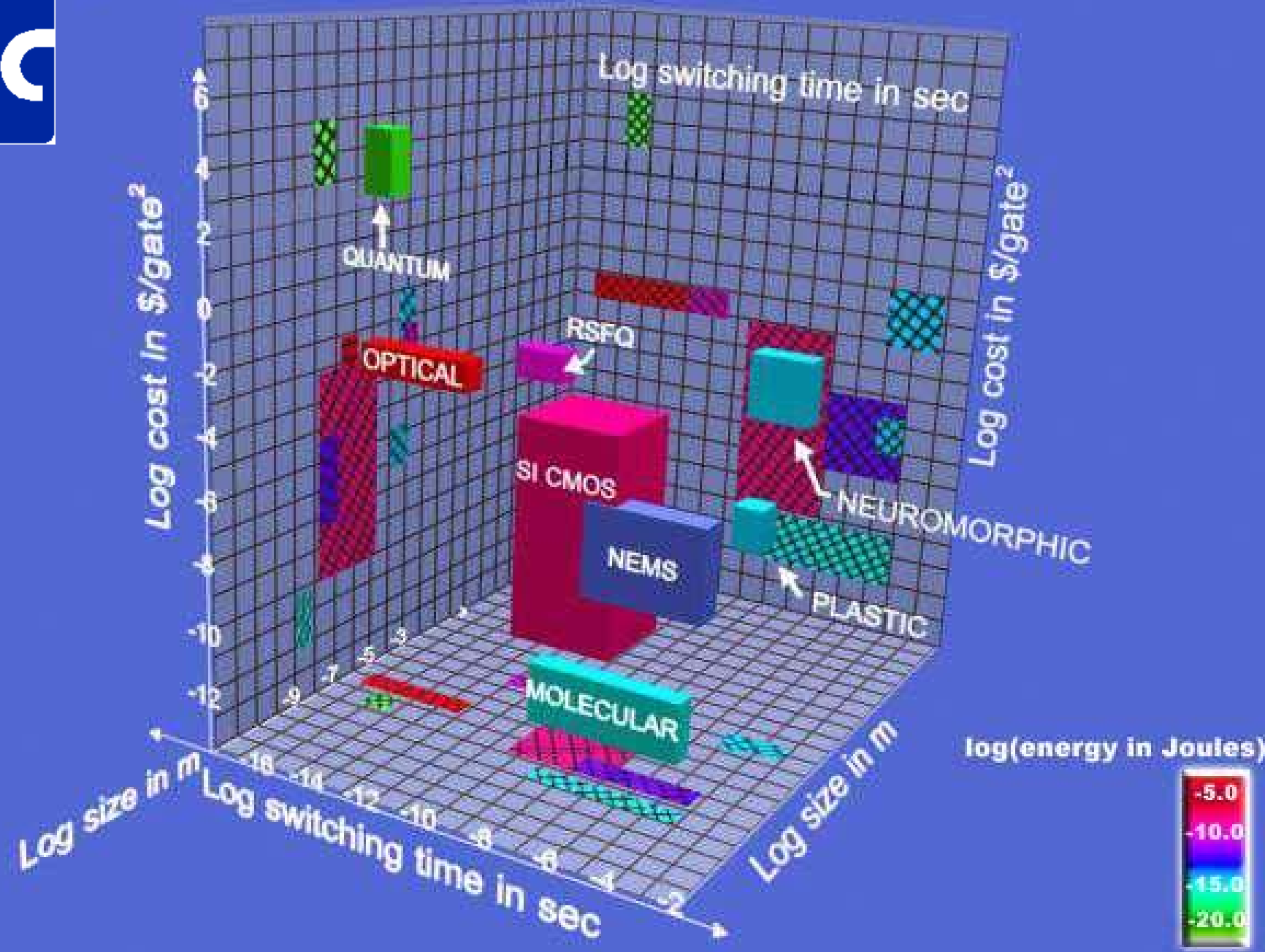
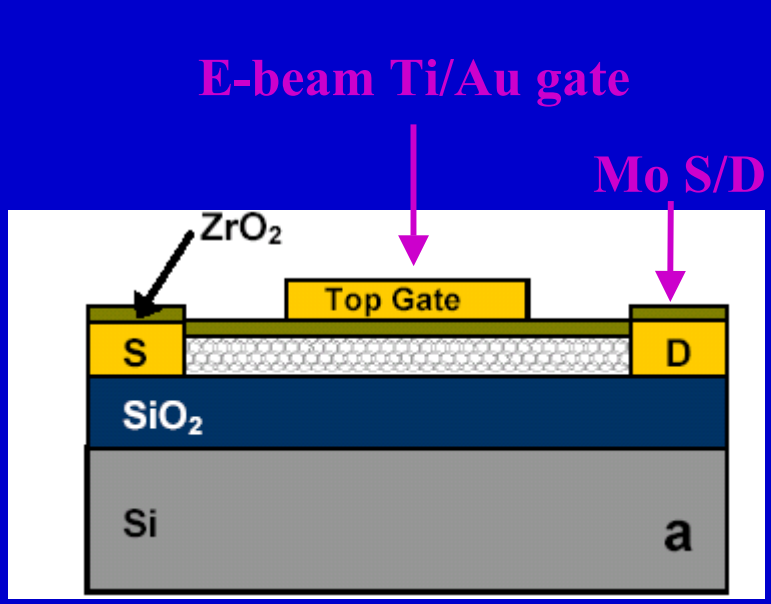
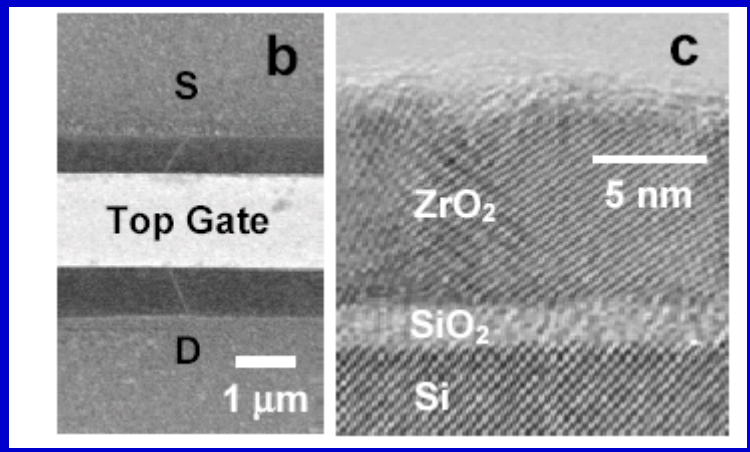
Emerging Technology Parametrization



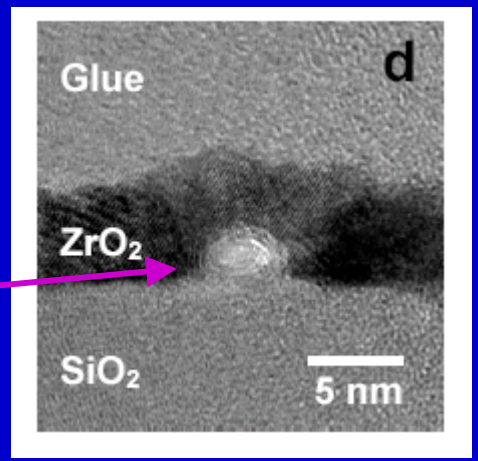
CNT-FET Device Structure





8 nm ZrO2

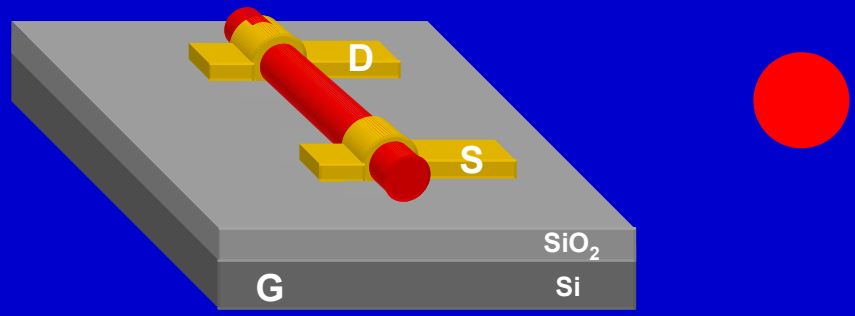
1.4 nm diameter single wall CNT



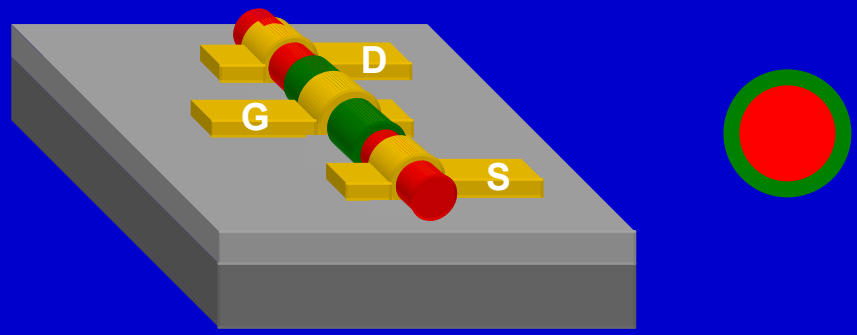
McEuen et. al, . Cornell Universwity

Nanowire Gating Geometries

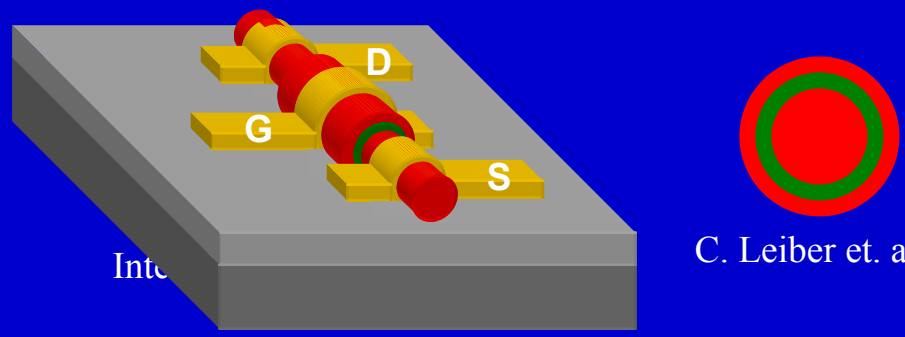
Back gate



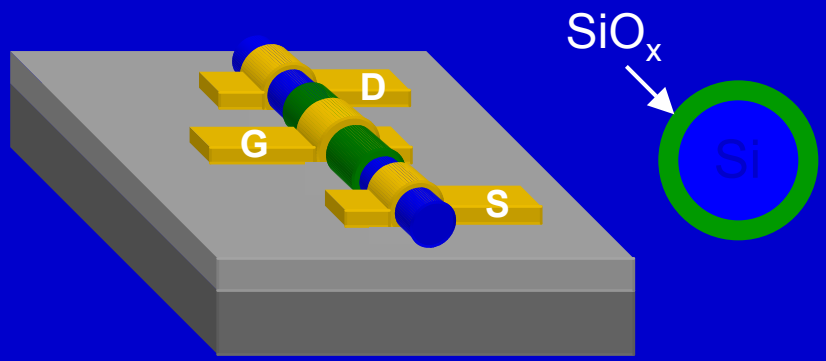
Top gate



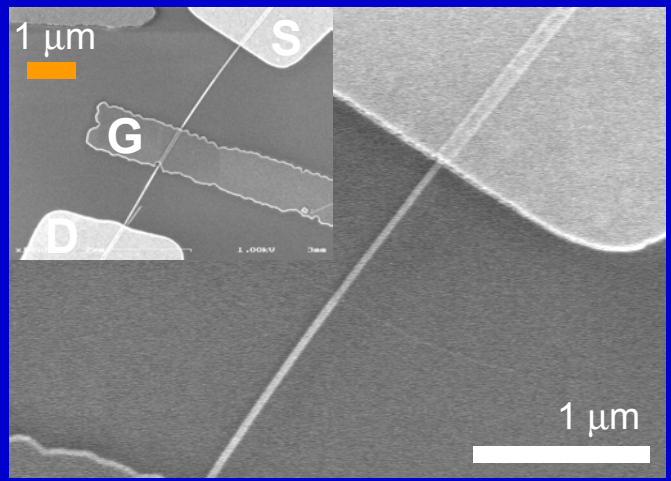
Coaxial gate

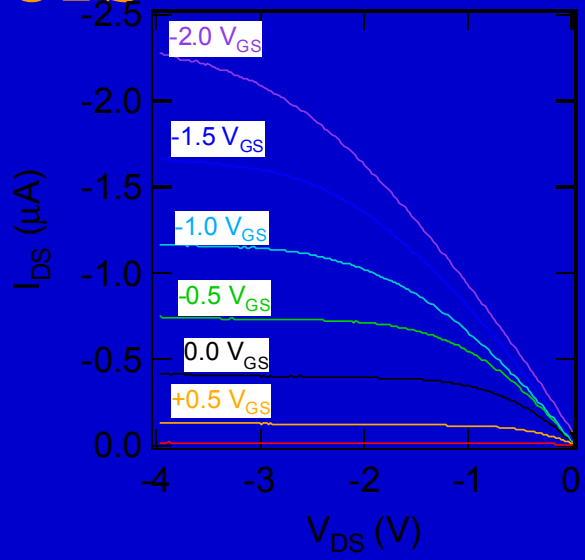


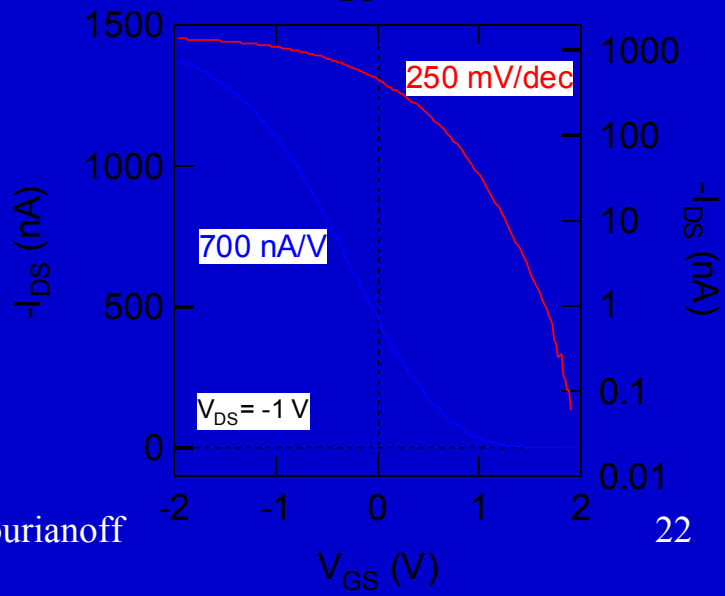
Top-gated p-Si Nanowire Transistors



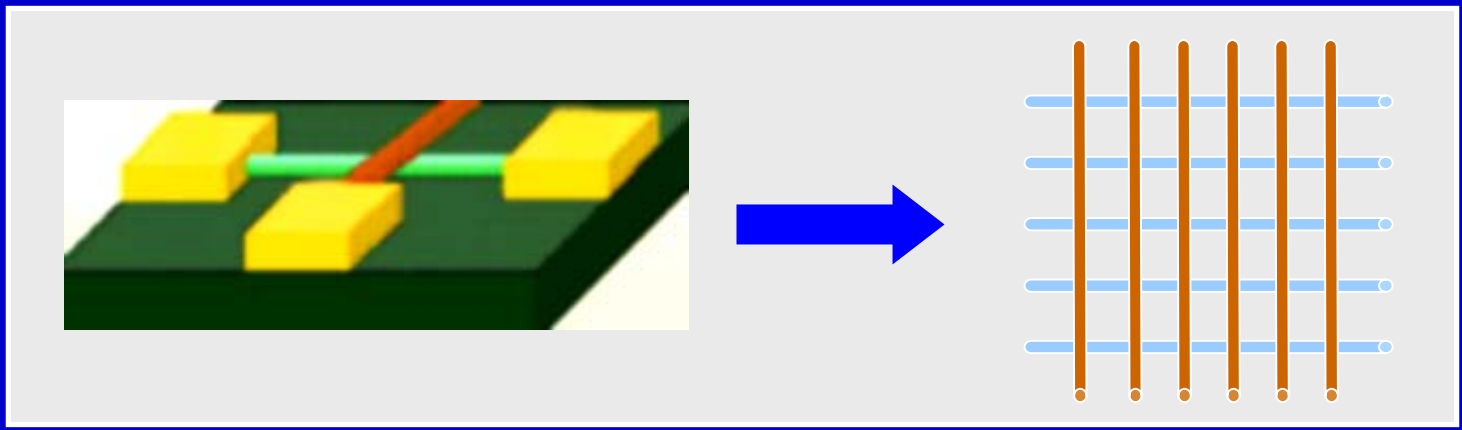
C. Leiber et. al. , Harvard U







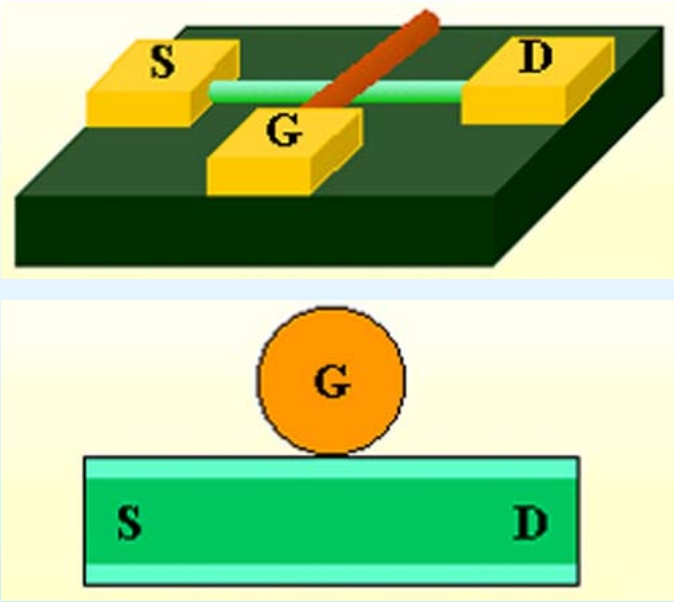
Crossed Nanowire Structures: A Powerful Strategy for Creation & Integration of Nanodevices

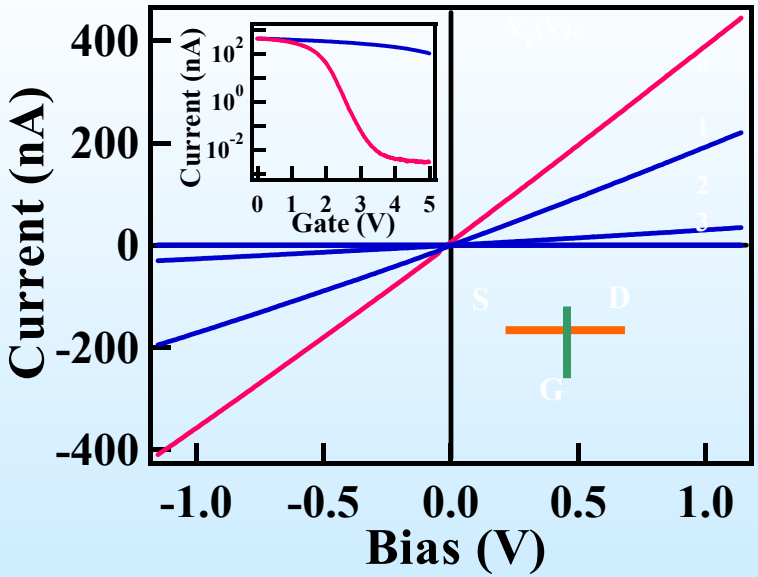


- Nanowires serve dual purpose: both active devices and interconnects.
- All key nanoscale metrics are defined during synthesis and subsequent assembly.
- Crossed nanowire architecture provides natural scaling and potential for integration at highest densities.
- No additional complexity (with added material).

C. Leiber et. al. , Harvard U

Crossed Nanowire FETs



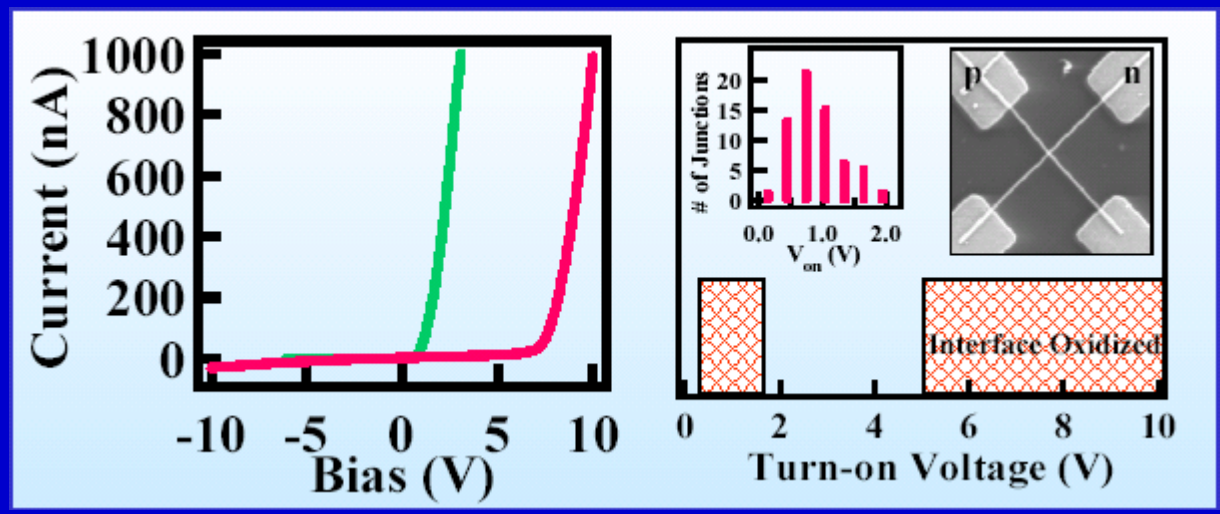


- In crossed nanowire FETs (cNW-FET), all critical nanoscale metrics are defined by synthesis and assembly:
  - channel width by the active nanowire diameter (to 2 nm)
  - channel length by the gate nanowire diameter (to 1-2 nm)
  - gate dielectric oxide coating on the nanowires (to 1 atomic layer)
- The conductance of cNW-FETs can be changed by more than 10^5-times with less than 0.1 V variation in the nano-gate.

Huang, Duan, Lieber et al., *Science* **294**, 1313 (2001)

Device Demonstrated

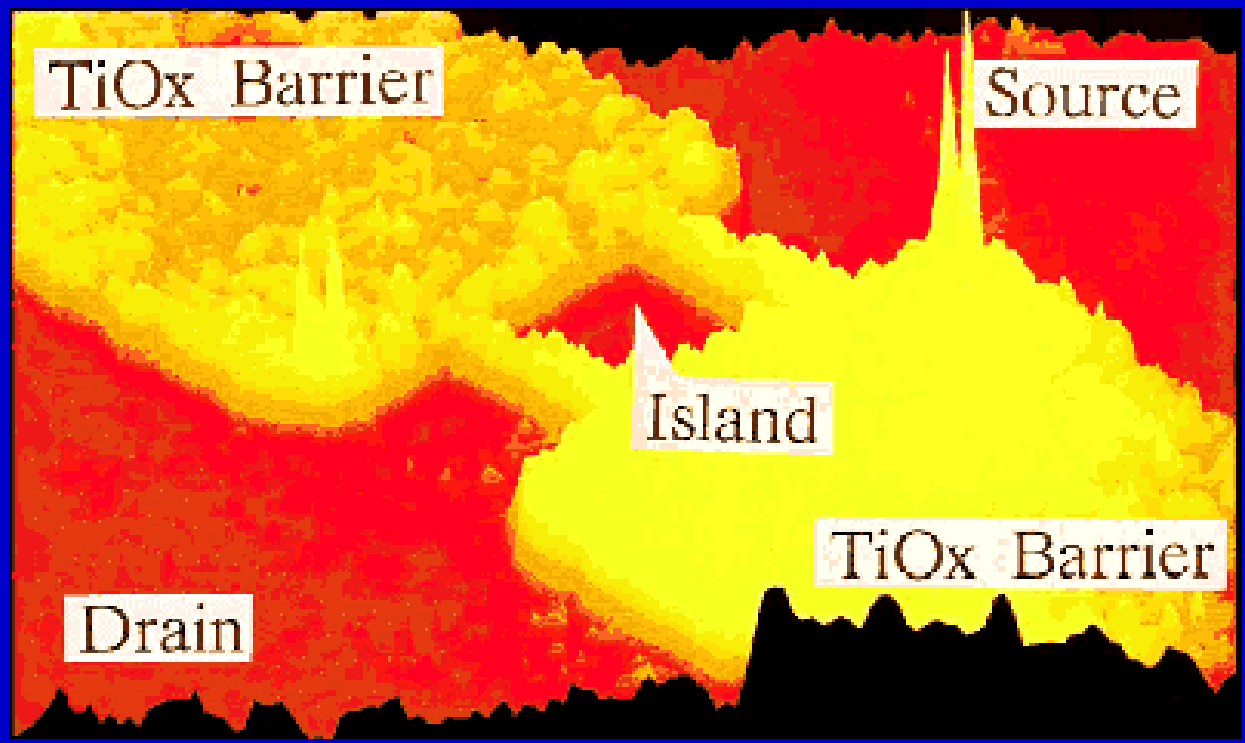
P-N Junction



Lieber/Harvard

Room temperature Single Electron Transistor (SET)

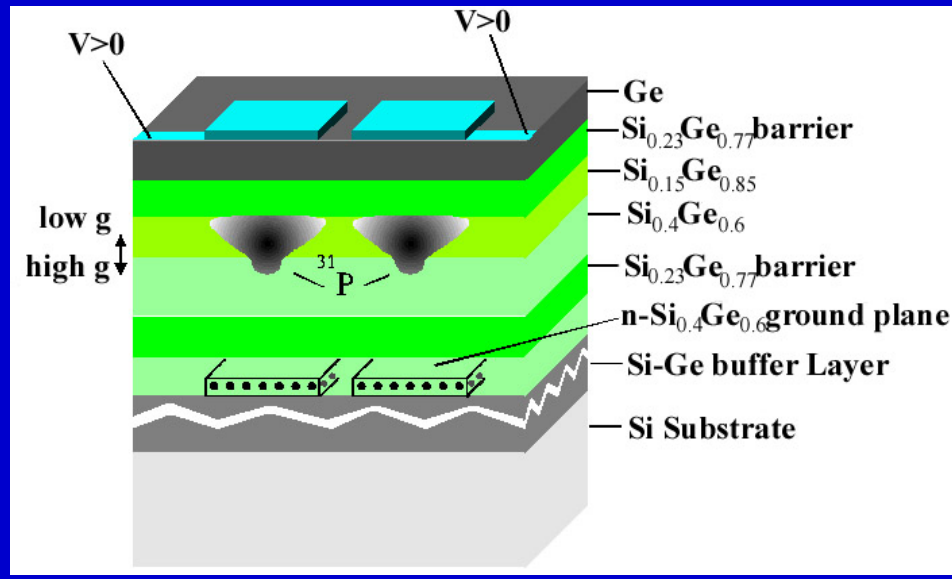
- Single electron in "island" controls current flow from source to drain
- Typical sizes of the TiOx lines are 15-25 nm widths and 30-50 nm lengths.
- Typical island sizes are 30-50 nm by 35-50 nm



Courtesy, NEC, IEDM 2000, PP 481

Spin resonance transistor (SRT)

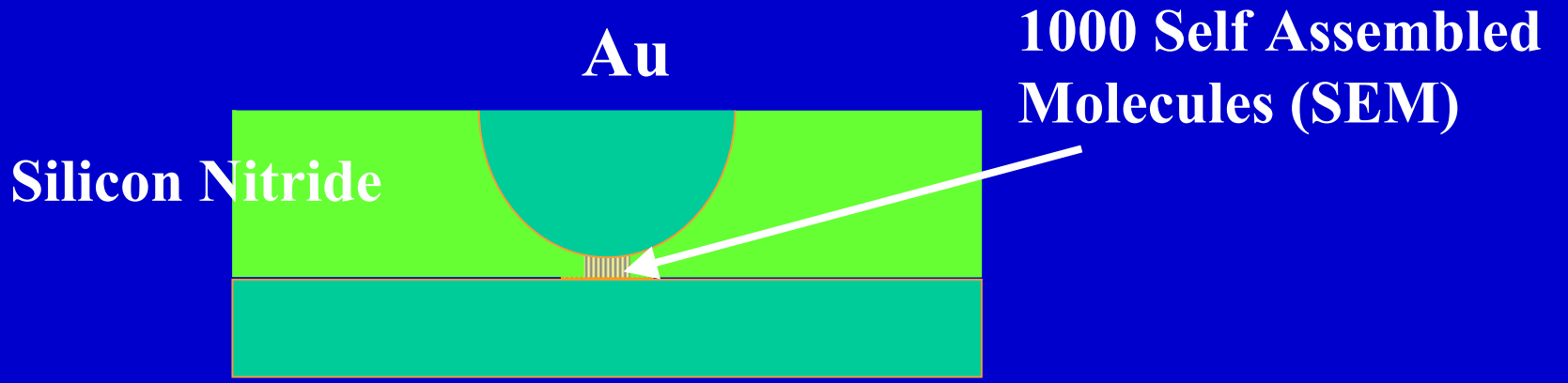
- Transistors that control spins rather than charge
- More energy efficient than conventional transistors
- Combines magnetic and electrostatic fields
- May enable quantum computing

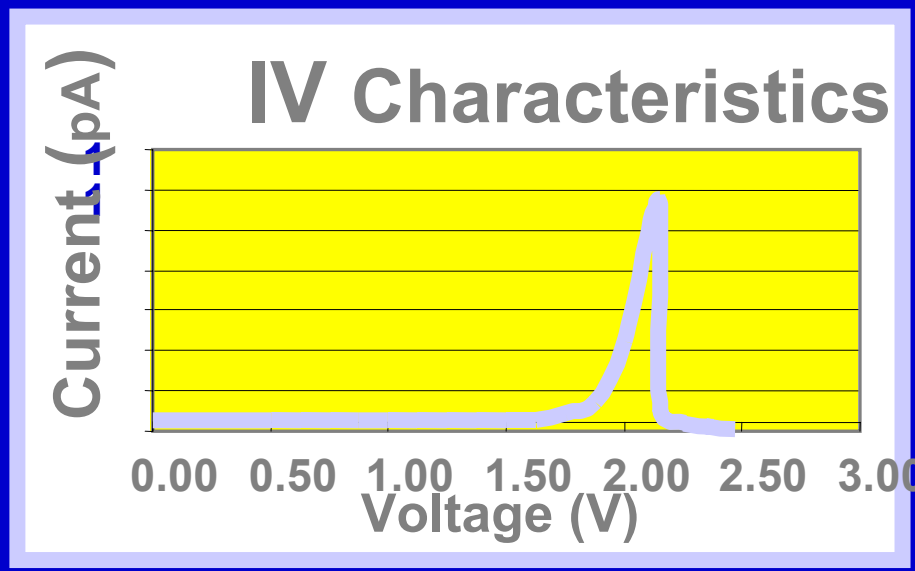


Courtesy Eli Yablanovitch, UCLA

A Molecular Electronic Switch

(2-amino-4-ethyinylphenyl-4-ethylphenyl-5-nitro-1-benzenethiolate)





(@T=60K)

Source: M.Reed & others,Yale Univ and Rice Univ

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  - **New devices**
  - **New architectures**
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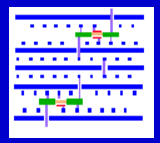
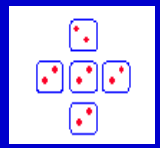
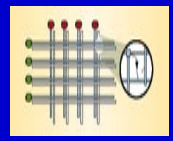
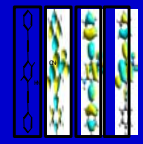
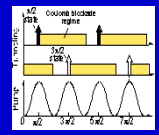
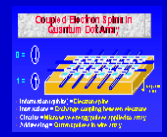
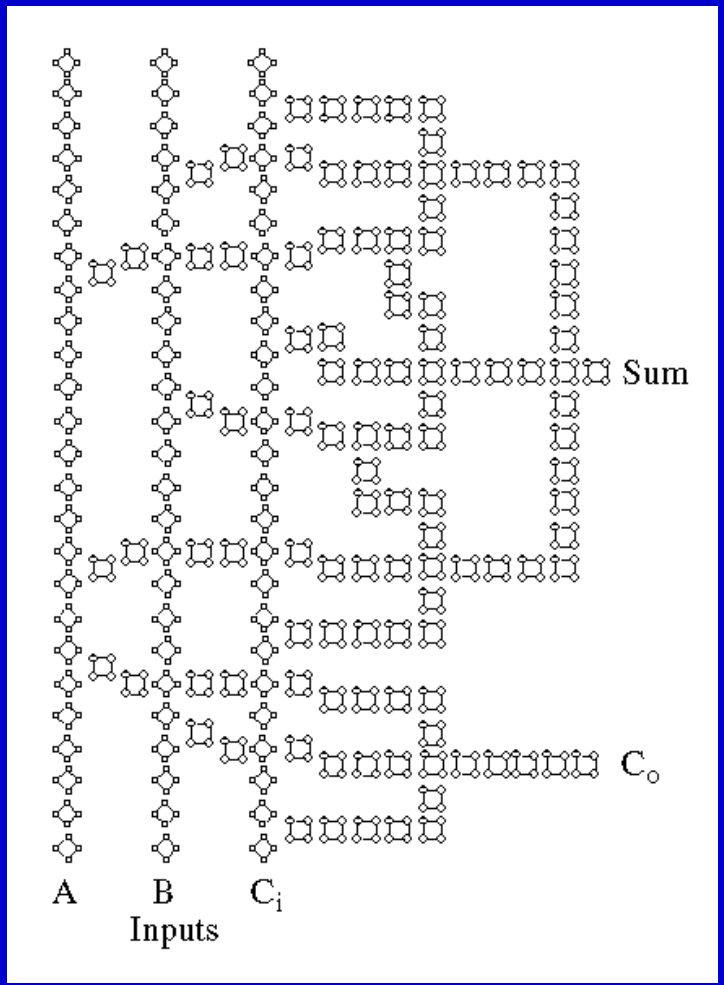
Emerging Research Architectures

						
Architecture	3-D Integration	Quantum Cellular Automata	Defect Tolerant Architecture	Molecular Architecture	Cellular Nonlinear Networks	Quantum Computing
Device Implementation	**CMOS with dissimilar material systems**	**Arrays of quantum dots**	**Intelligently assembles nanodevices**	**Molecular switches and memories**	**Single electron array architectures**	**Spin resonance transistors, NMR devices, Single flux quantum devices**
Advantages	**Less interconnect delay, Enables mixed technology solutions**	**High functional density. No interconnects in signal path**	**Supports hardware with defect densities >50%**	**Supports memory based computing**	**Enables utilization of single electron devices at room temperature**	**Exponential performance scaling, Enables unbreakable cryptography**
Challenges	**Heat removal, No design tools, Difficult test and measurement**	**Limited fan out, Dimensional control (low temperature operation), Sensitive to background charge**	**Requires pre-computing test**	**Limited functionality**	**Subject to background noise, Tight tolerances**	**Extreme application limitation, Extreme technology**
Maturity	**Demonstration**	**Demonstration**	**Demonstration**	**Concept**	**Demonstration**	**Concept**

Quantum Cellular Automata

Adder circuit with carry executed in QCA logic

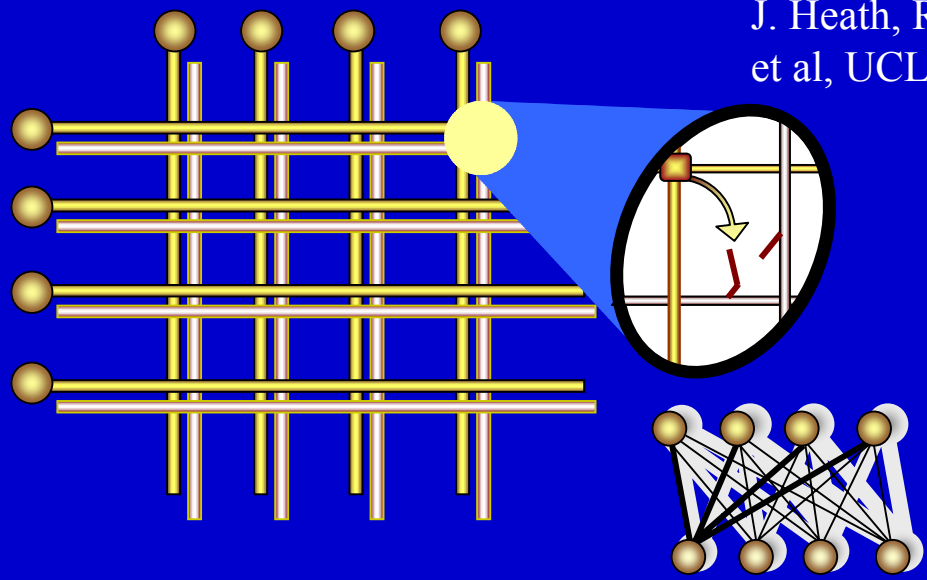
Example of asynchronous, CNN, nearest neighbor architecture



Courtesy of Notre Dame

Fault tolerant architecture

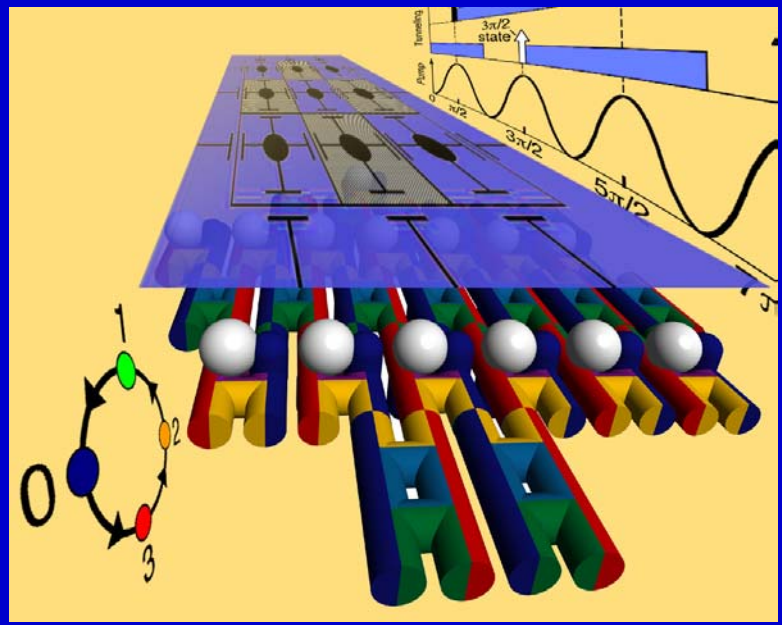
- All-memory architecture
- Defect tolerant
- Potentially self-repairing and reconfigurable



J. Heath, R. S. Williams et al, UCLA and HP

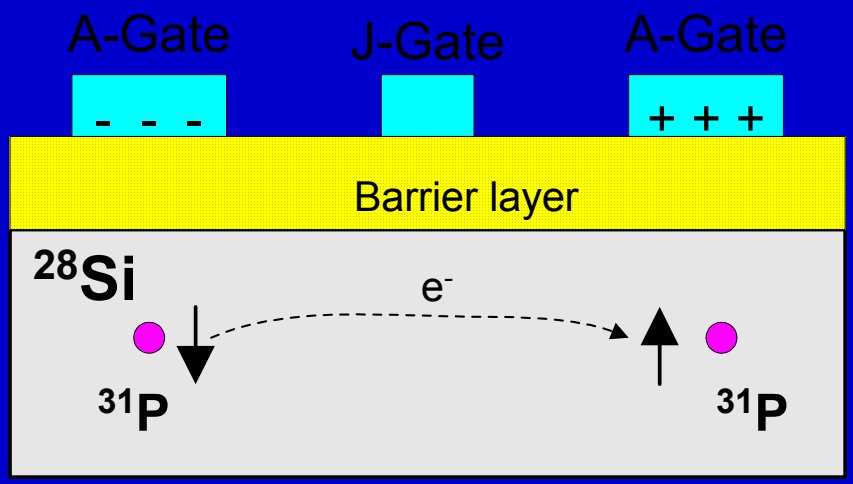
Phase logic

- Store information in the relative phase of 2 signals
- Multi-valued logic possible depending on frequencies of 2 signals
- Tunneling Phase logic devices use RTDs to create one of the signals



Courtesy: R Keihle, University of Minnesota

Quantum Computer



Selected technological implementations

- Liquid-state NMR
- Linear ion trap
- Coupled quantum dots
- ***Deterministically doped semicondustor structures***

The future of nanocomputing

- Introduction
- Scaled CMOS
- **Nano-computing, nano-technology and nano-science**
  - A taxonomy
  - New devices
  - New architectures
  - **Alternative state variables**
- Radical new technologies
- Challenges
- Conclusions

Alternative state variables

- Electric charge
- Molecular state
- Spin orientation
- Electric dipole orientation
- Photon intensity
- Photon polarization
- Quantum state
- Phase state
- Mechanical state

The future of nanocomputing

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Economic criteria

- Economic relevance criteria
  - The risk adjusted ROI for any new technology must exceed that of silicon
- Caution
  - Sufficiently advanced technologies will create their own applications. New technologies cannot necessarily be justified by current day applications.

Technical criteria

- ***CMOS compatibility***
- ***Energy efficiency***
- ***Scalability***
- ***Performance***
- ***Architectural compatibility***
- ***Sensitivity to parametric variation***
- ***Room temperature operation***
- ***Stability and reliability***

Existence proof for alternate models

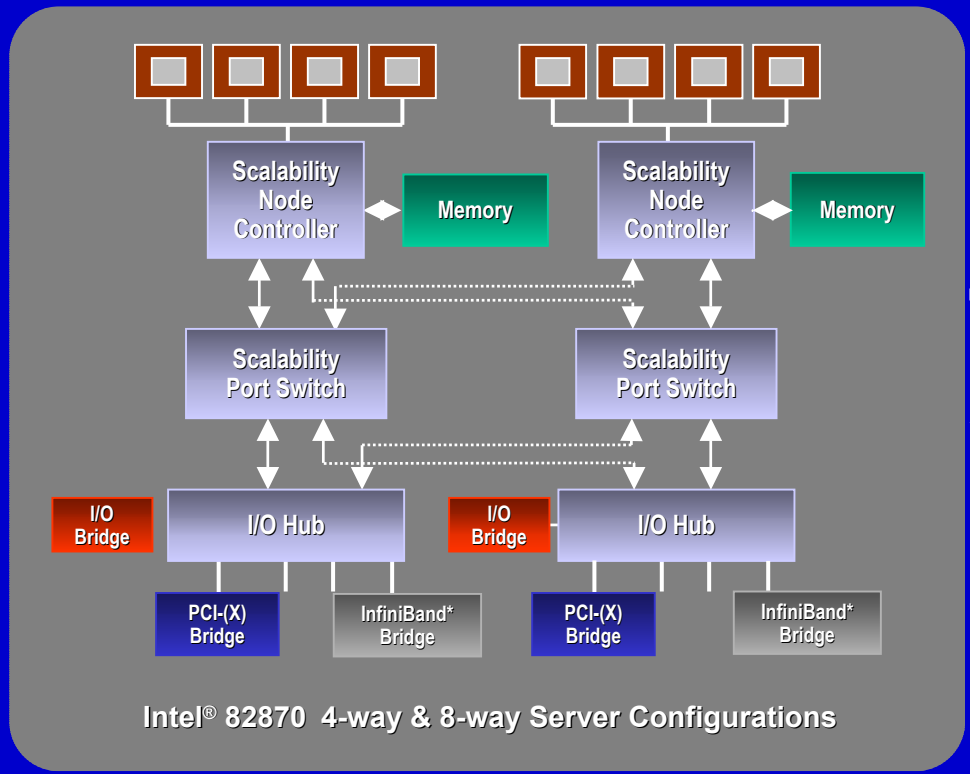
The brain is the ultimate model for its ability to deal with complexity

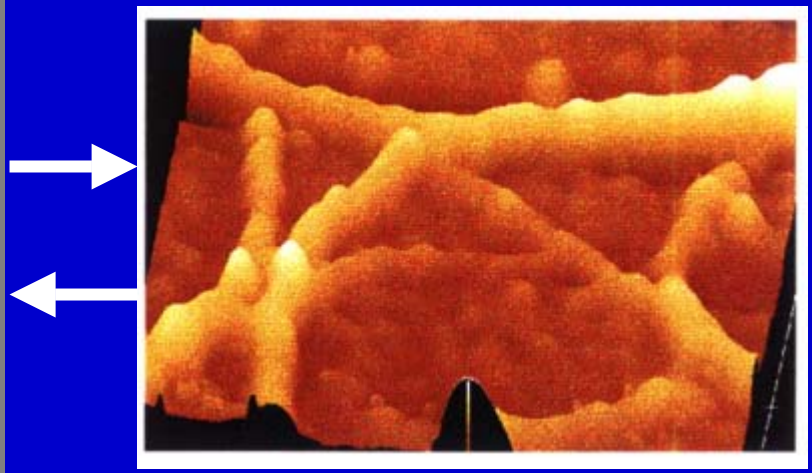
- Little understanding on its architecture & organization
- It is however
  - Orders of magnitude more powerful than the best microprocessor
  - Self assembled
  - Parallel operation
  - Self repairing to a significant degree
  - Fault tolerant
  - Runs on ~ 10W

Breakthrough scientific investigation is needed

1952 Achievements	*2002 Needs*
• ***Bulk* band structure of solids**	• **geometry dependent energetic structure of nanostructures**
• **Doping**	• **precise location of atoms**
• **Crystal growth**	• **self organization of matter in complex structures**

The integration challenge



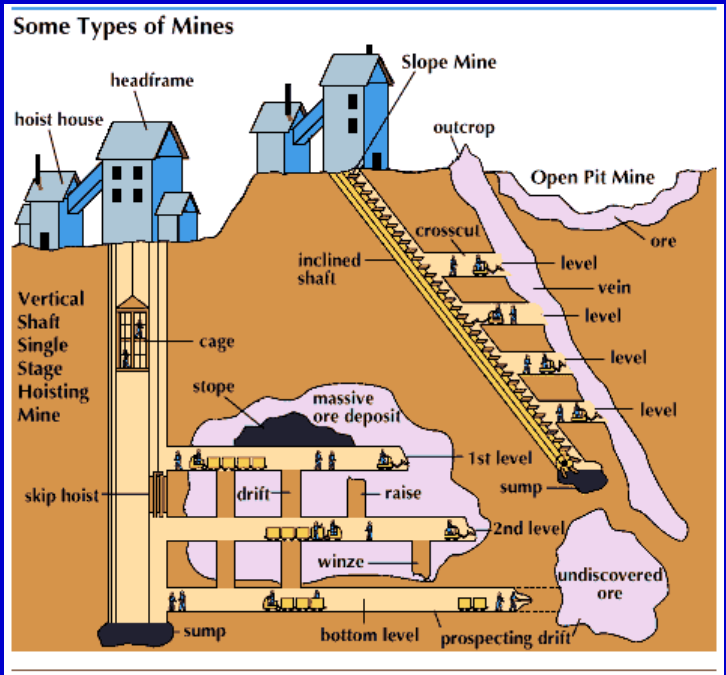


Conclusions

- CMOS scaling will continue for next 12 –15 years
- Alternative new technologies will emerge and begin to be integrated on CMOS by 2015
- Nanoscience research is needed to facilitate radical new scalable technologies beyond 2020

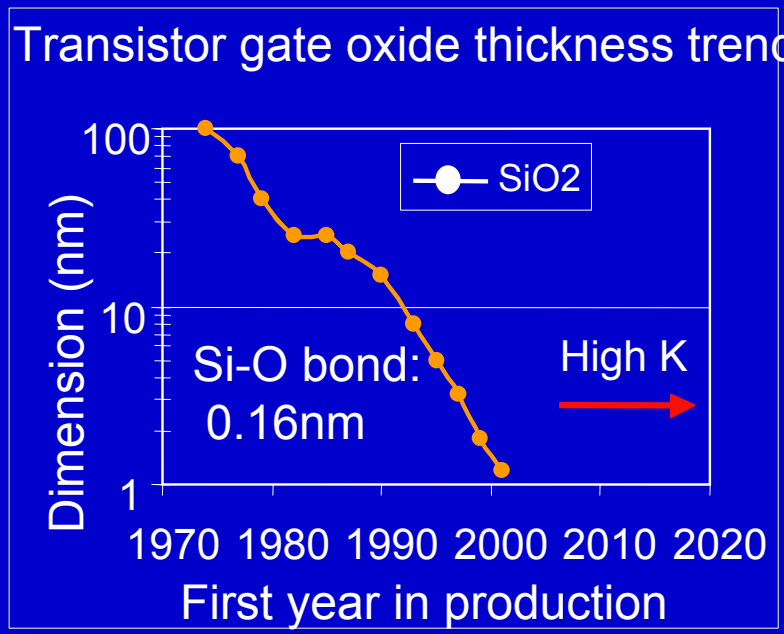
For further information on Intel's silicon technology, please visit the Silicon Showcase at www.intel.com/research/silicon

Backup



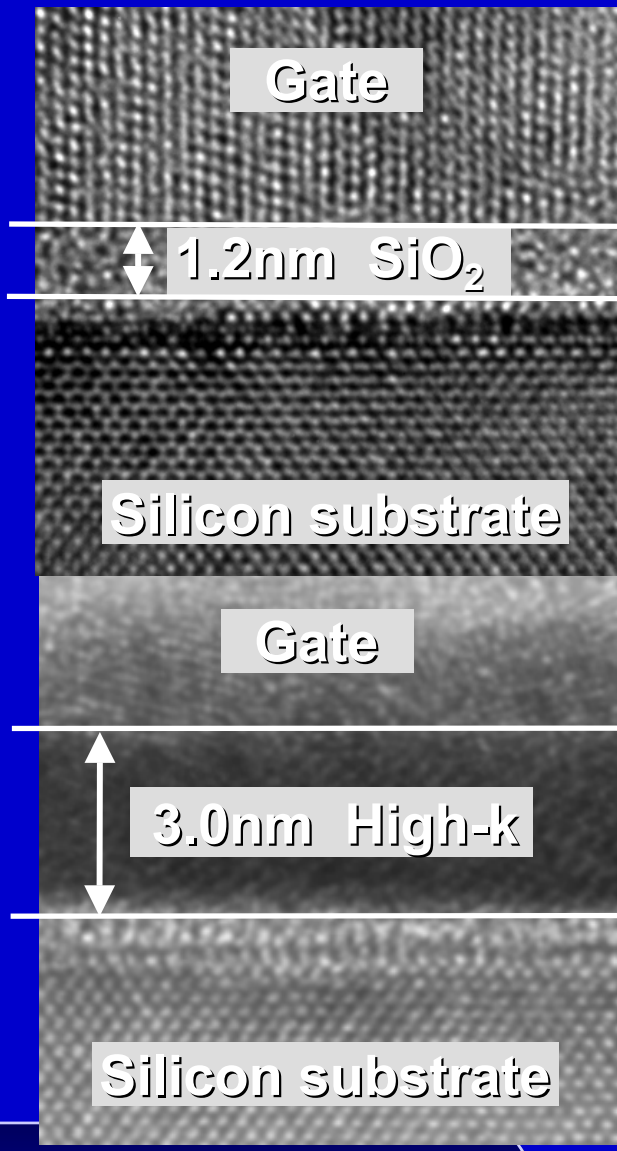
For about four decades now we have exploited (mined) our investment in basic science and we have continuously evolved the devices based on this understanding

Nanotechnology for Gate Dielectrics



Source: Intel

	90nm process	Experimental high-k
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

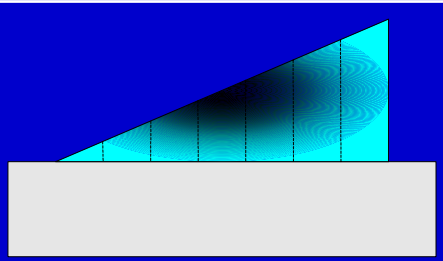


Leakage is the limiter to SiO2 scaling
Integration is the key challenge to High K

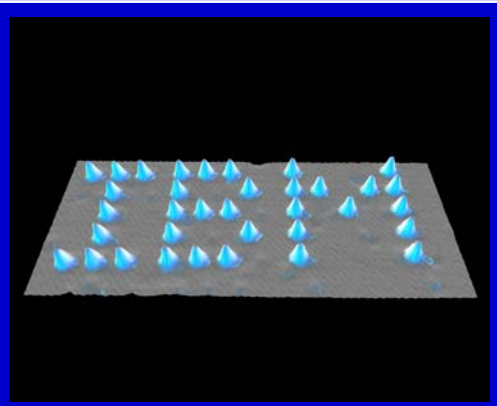
What new basic science is needed?

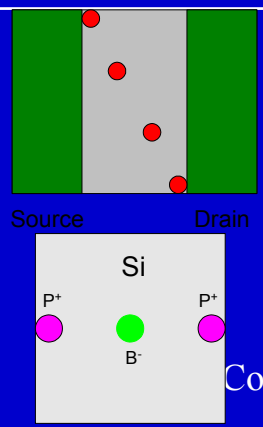
$$\vec{S} \rightarrow R$$

- *Spin manipulation*, e.g. transport, storage, detection, creation, …



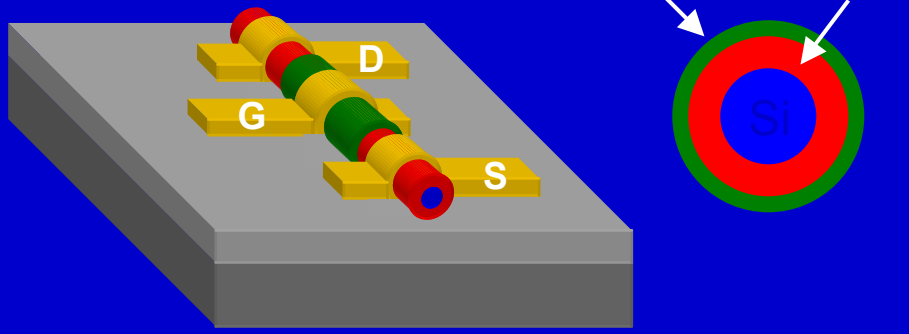
- *Geometry related quantum effects*, e.g. quantum wedge, parabolic wells, …

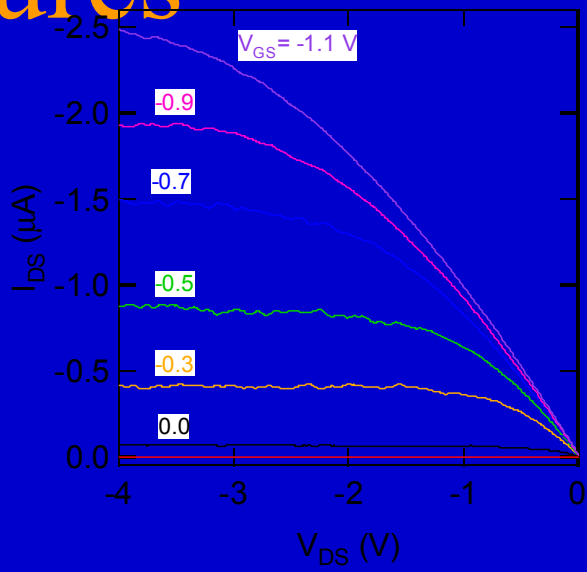


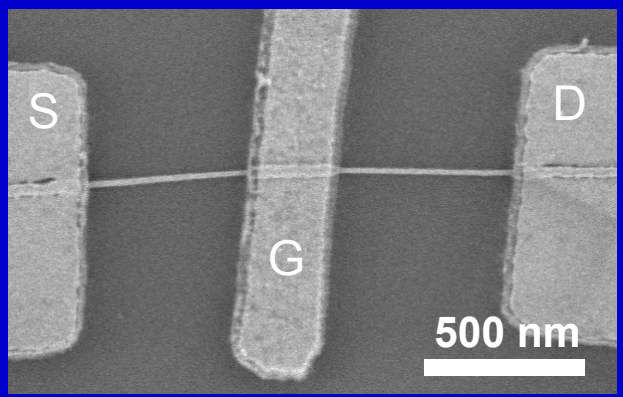


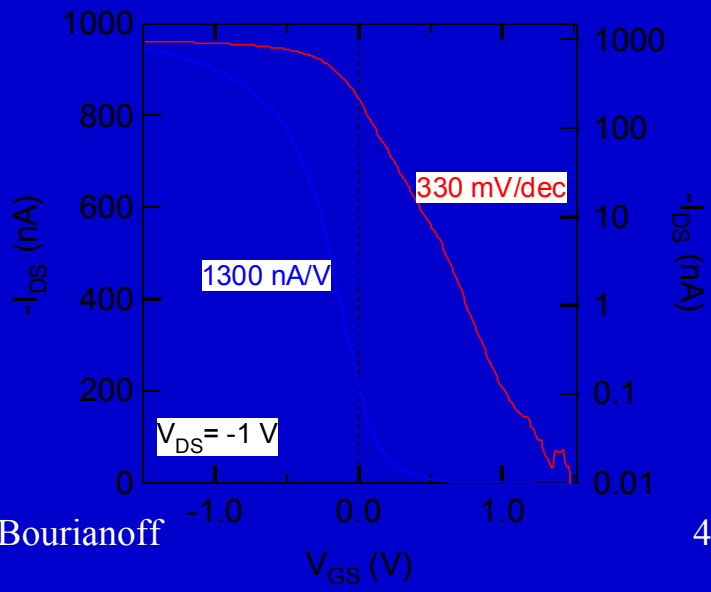
- *Precise location of atoms* e.g. coherent manipulation of entangled wavefunctions

Transport in Si-Ge Core-Shell Structures

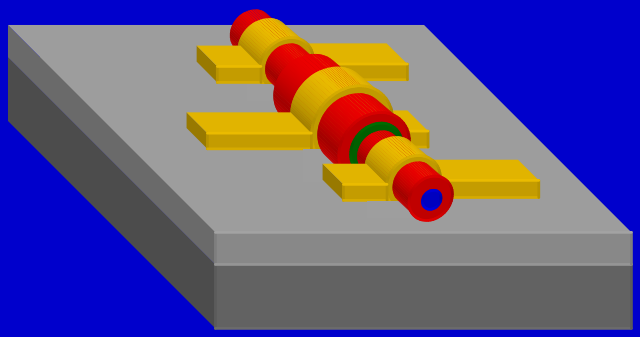


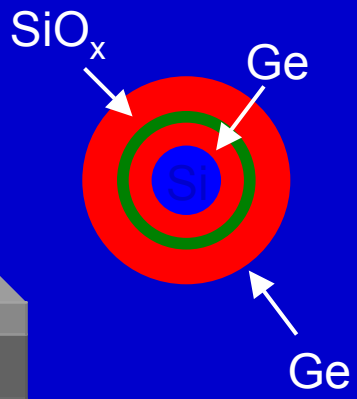


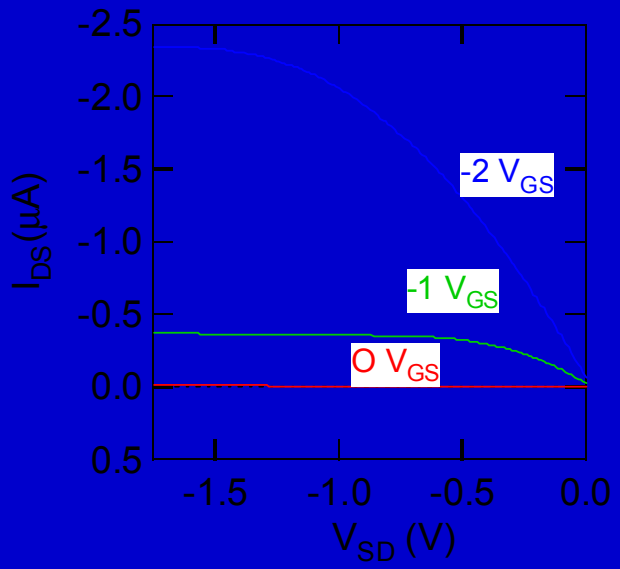


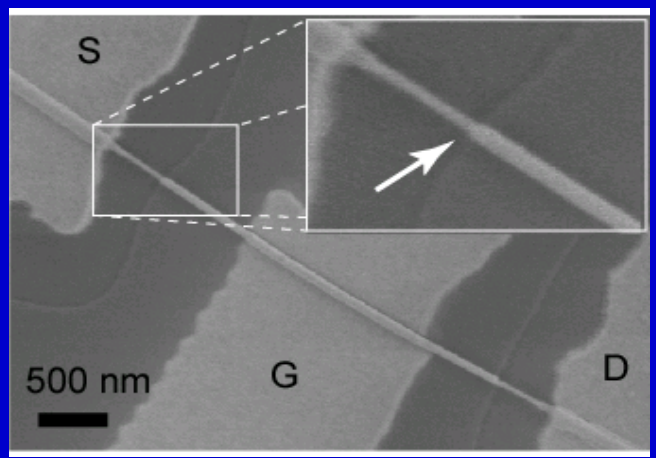


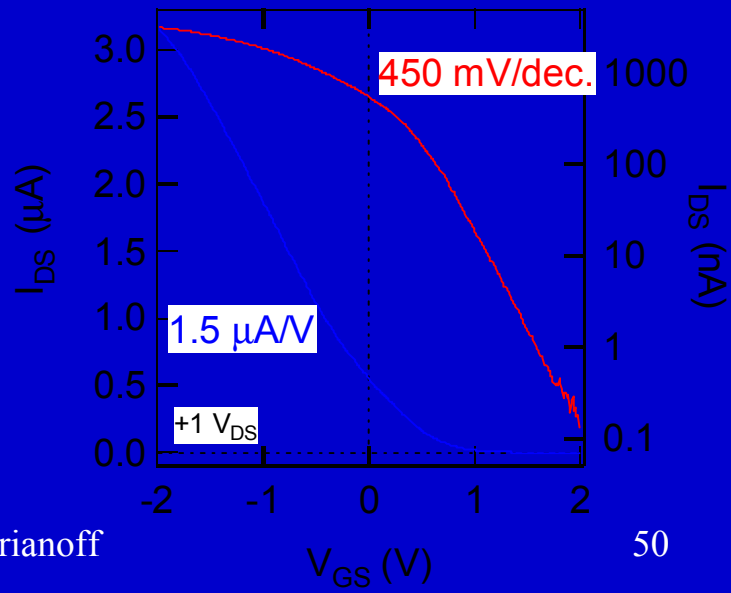
Coaxially-Gated Si-Ge





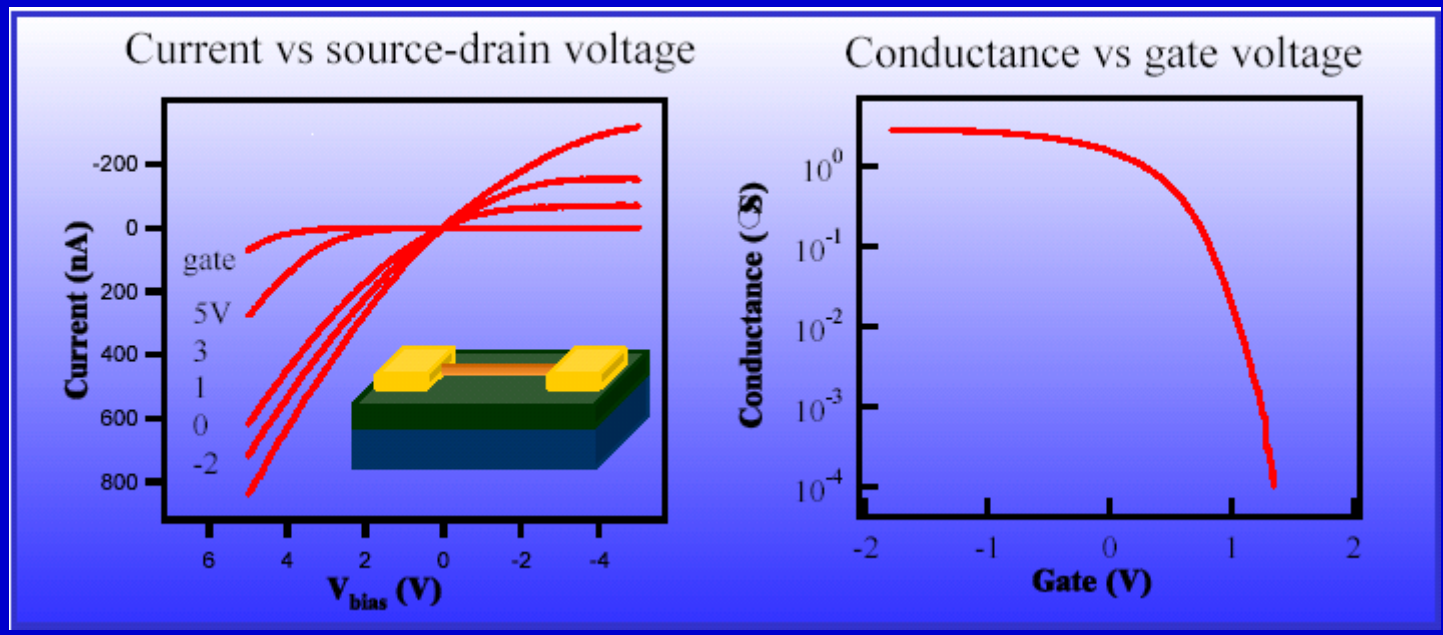






Devices Demonstrated

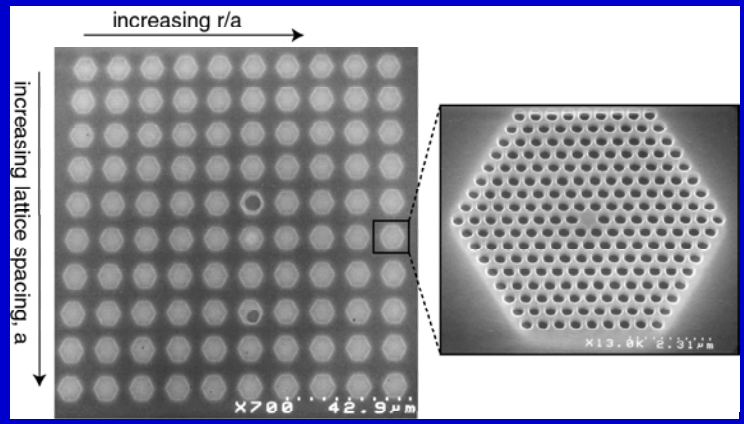
Nanowire FET

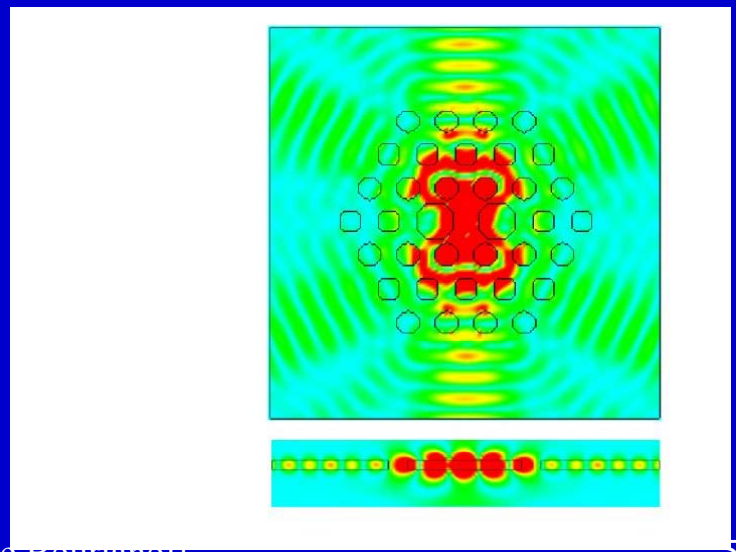


Lieber/Harvard

Photonic devices

- Man-made crystals produced by etching precisely placed holes in silicon or III-V material
- Can produce, detect and manipulate light more efficiently than naturally occurring materials





System software design needs to facilitate emerging technologies

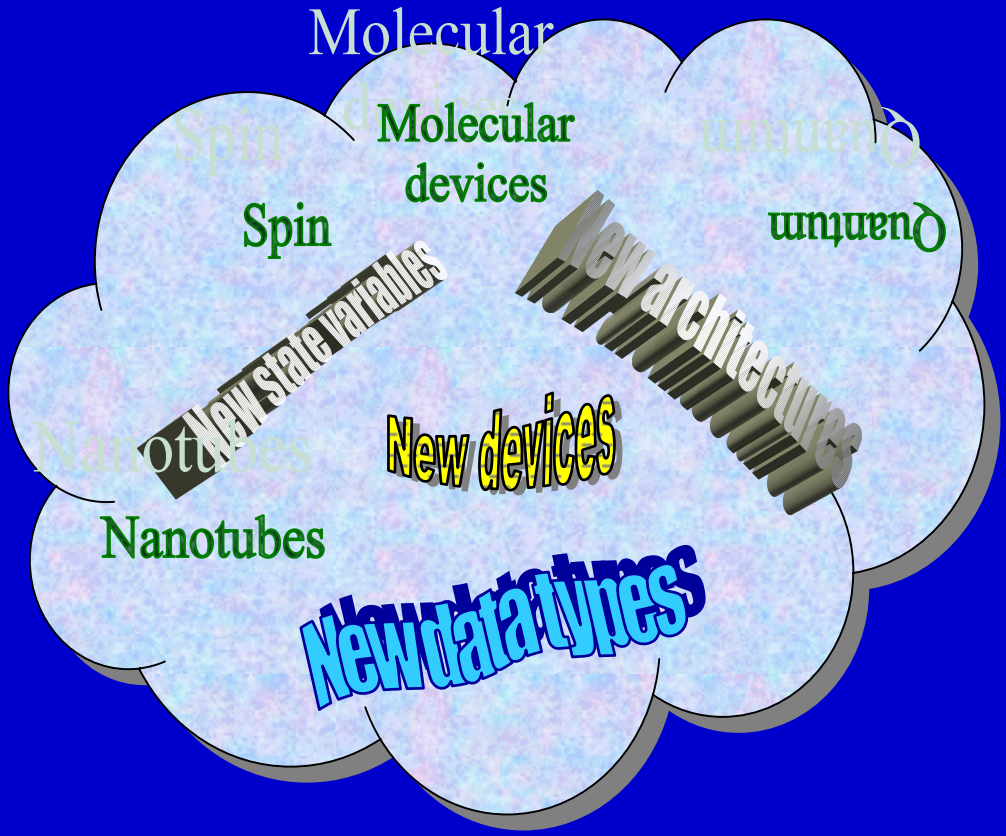
Challenge

- CMOS is based on Boolean logic and binary data representation
- Alternative technologies will require "native" logic systems and data representations to optimize their performance

Solution?

- Design science must provide functional abstractions and interfaces to couple multiple, dissimilar technologies into a single functional system

Nano-computing, nano-technology and nano-science



Changing architectural paradigms

Current	Future
• Boolean logic	• Neural networks, CNN, QCA,…
• Binary data representation	• Associative, patterned, memory based, … data representations
• 2D	• 3D
• Homogeneous	• Non homogeneous
• Globally interconnected	• Nearest neighbor
• Synchronous	• Asynchronous
• Von Neuman	• Integrated memory/logic
• 3 terminal	• 2 terminal